1Gb(64Mx16) DDR2 SDRAM

H5PS1G63EFR

Revision History

Revision	Page	History	Date	Remark
0.1	All	Initial data sheet released. -.500Mhz characteristics inserted.	May. 2008	Preliminary
0.2	5	500Mhz@2.0 Part Number deleted.	Jul. 2008	Preliminary
	61	IDD value(-25C) inserted.		
0.3	64,67	IDD testing parameters' value edited.	Jul. 2008	Preliminary
0.4	56	Operating temperature condition changed.	Aug. 2008	Preliminary
1.0	62	IDD Value(-20L) inserted.	Aug. 2008	
	56	Thermal resistance value inserted.		
1.1	69	Typo corrected. (500Mhz tWR Value)	Oct. 2008	

Note) The H5PS1G63EFR data sheet follows all of JEDEC DDR2 standard.

Contents

1. Description

1.1 Device Features & Ordering Information

1.1.1 Key Features

- VDD = 1.8 +/- 0.1V
- VDDQ = 1.8 +/- 0.1V
- All inputs and outputs are compatible with SSTL_18 interface
- 8 banks
- Fully differential clock inputs (CK, /CK) operation
- Double data rate interface
- Source synchronous-data transaction aligned to bidirectional data strobe (DQS, $\overline{DQS}$)
- Differential Data Strobe (DQS, $\overline{DQS}$)
- Data outputs on DQS, $\overline{DQS}$ edges when read (edged DQ)
- Data inputs on DQS centers when write(centered DQ)
- On chip DLL align DQ, DQS and $\overline{DQS}$ transition with CK transition
- DM mask write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable CAS latency 3,4, 5, 6 and 7 supported
- Programmable additive latency 0, 1, 2, 3, 4 and 5 supported
- Programmable burst length 4/8 with both nibble sequential and interleave mode
- Internal eight bank operations with single pulsed RAS
- Auto refresh and self refresh supported
- tRAS lockout supported
- 8K refresh cycles /64ms
- JEDEC standard 84ball FBGA(x16)
- Full strength driver option controlled by EMR
- On Die Termination supported
- Off Chip Driver Impedance Adjustment supported
- Read Data Strobe supported (x8 only)
- Self-Refresh High Temperature Entry
- Average Refresh Period 7.8us at lower than Tcase 85°C, 3.9us at 85°C<Tcase<95°C

1.1.2 Ordering Information

Part No.	Power Supply	Clock Frequency	Max Data Rate	Interface	Package
H5PS1G63EFR-20L	VDD/VDDQ=1.8V	500Mhz	1000Mbps/pin	SSTL_18	84Ball FBGA
H5PS1G63EFR-25C		400Mhz	800Mbps/pin		

Note) Above Hynix P/N's are Lead-free, RoHS Compliant and Halogen-free.

1.2 Pin configuration

64Mx16 DDR2 PIN CONFIGURATION(Top view: see balls through package)

1	2	3		7	8	9
VDD	NC	VSS	A	VSSQ	$\overline{\text{UDQS}}$	VDDQ
DQ14	VSSQ	UDM	B	UDQS	VSSQ	DQ15
VDDQ	DQ9	VDDQ	C	VDDQ	DQ8	VDDQ
DQ12	VSSQ	DQ11	D	DQ10	VSSQ	DQ13
VDD	NC	VSS	E	VSSQ	$\overline{\text{LDQS}}$	VDDQ
DQ6	VSSQ	LDM	F	LDQS	VSSQ	DQ7
VDDQ	DQ1	VDDQ	G	VDDQ	DQ0	VDDQ
DQ4	VSSQ	DQ3	H	DQ2	VSSQ	DQ5
VDDL	VREF	VSS	J	VSSDL	CK	VDD
	CKE	$\overline{\text{WE}}$	K	$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT
NC, BA2	BA0	BA1	L	$\overline{\text{CAS}}$	$\overline{\text{CS}}$	
	A10/AP	A1	M	A2	A0	VDD
VSS	A3	A5	N	A6	A4	
	A7	A9	P	A11	A8	VSS
VDD	A12	NC, A14	R	NC, A15	NC, A13	

ROW AND COLUMN ADDRESS TABLE

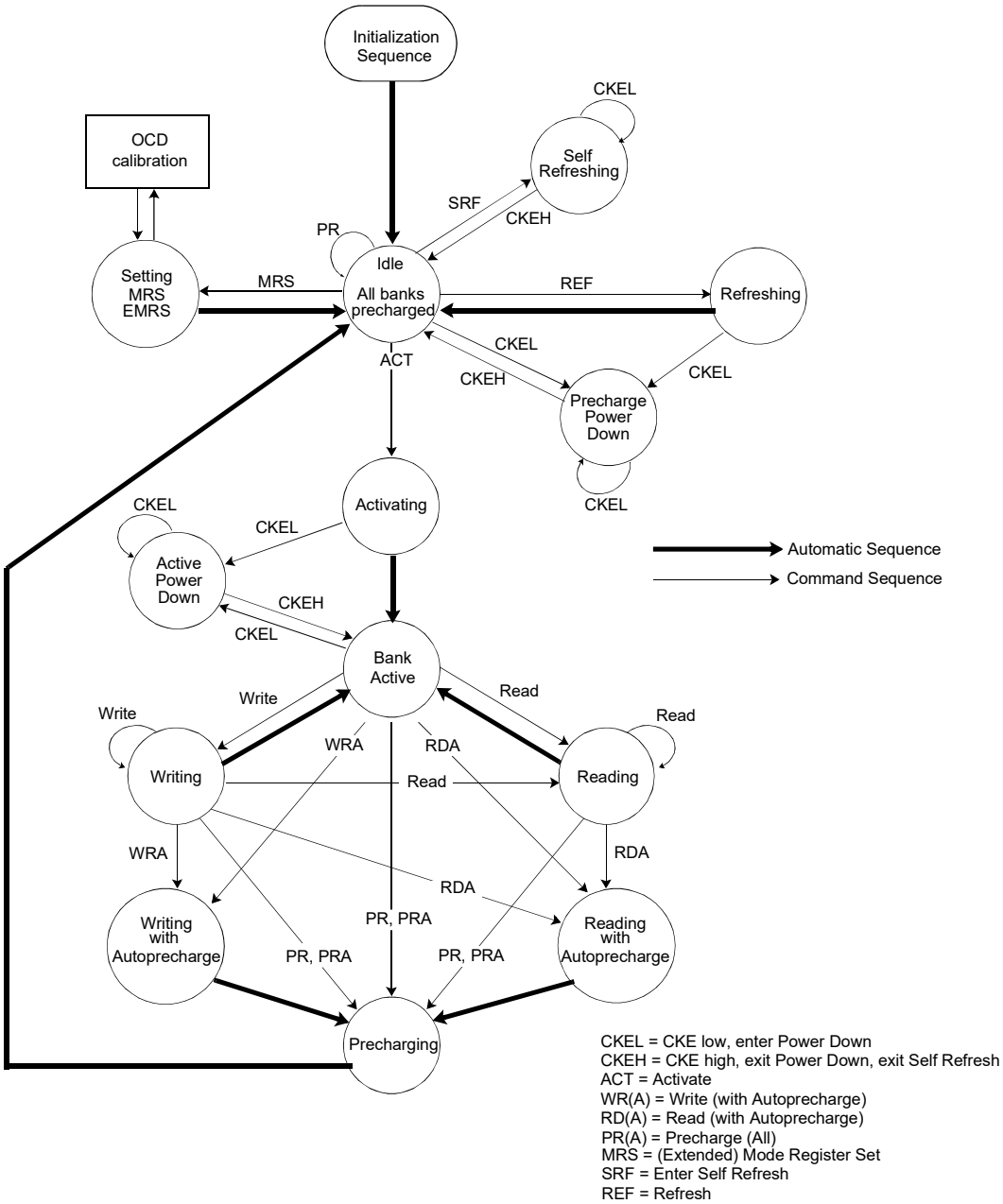
ITEMS	64Mx16
# of Bank	8
Bank Address	BA0, BA1, BA2
Auto Precharge Flag	A10/AP
Row Address	A0 - A12
Column Address	A0-A9
Page size	2 KB

1.3 PIN DESCRIPTION

PIN	TYPE	DESCRIPTION
CK, $\overline{CK}$	Input	**Clock**: CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE	Input	**Clock Enable**: CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank). CKE is synchronous for POWER DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit. After V_{REF} has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, V_{REF} must be maintained to this input. CKE must be maintained HIGH throughout READ and WRITE accesses. Input buffers, excluding CK, $\overline{CK}$ and CKE are disabled during POWER DOWN. Input buffers, excluding CKE are disabled during SELF REFRESH.
$\overline{CS}$	Input	**Chip Select** : Enables or disables all inputs except CK, $\overline{CK}$, CKE, DQS and DM. All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. $\overline{CS}$ is considered part of the command code.
ODT	Input	**On Die Termination Control** : ODT(registered HIGH) enables on die termination resistance internal to the DDR2 SDRAM. When enabled, ODT is applied to each DQ, UDQS/$\overline{UDQS}$, LDQS/$\overline{LDQS}$, UDM and LDM signal. The ODT pin will be ignored if the Extended Mode Register(EMR(1)) is programmed to disable ODT.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs** : $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM (LDM, UDM)	Input	**Input Data Mask** : DM is an input mask signal for write data. Input Data is masked when DM is sampled High coincident with that input data during a WRITE access. DM is sampled on both edges of DQS, Although DM pins are input only, the DM loading matches the DQ and DQS loading.
BA0 - BA2	Input	**Bank Address Inputs** : BA0 - BA2 define to which bank an ACTIVE, Read, Write or PRECHARGE command is being applied(For 2Mb and 512Mb, BA2 is not applied). Bank address also determines if one of the mode register or extended mode register is to be accessed during a MR or EMR command cycle.
A0 -A12	Input	**Address Inputs** : Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands to select one location out of the memory array in the respective bank. A10 is sampled during a precharge command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0-BA2. The address inputs also provide the op code during MRS or EMRS commands.
DQ	Input/Output	**Data input / output** : Bi-directional data bus
(UDQS),($\overline{UDQS}$) (LDQS),($\overline{LDQS}$)	Input/Output	**Data Strobe** : Output with read data, input with write data. Edge aligned with read data, centered in write data. For the x16, LDQS correspond to the data on DQ0~DQ7; UDQS corresponds to the data on DQ8~DQ15. The data strobes LDQS & UDQS may be used in single ended mode or paired with optional complementary signals LDQS & UDQS to provide differential pair signaling to the system during both reads and wirtes. An EMR(1) control bit enables or disables all complementary data strobe signals. In this data sheet, "differential DQS signals" refers to any of the following with A10 = 0 of EMR(1) x16 LDQS/$\overline{LDQS}$ and UDQS/$\overline{UDQS}$ "single-ended DQS signals" refers to any of the following with A10 = 1 of EMR(1) x16 LDQS and UDQS
NC		**No Connect** : No internal electrical connection is present.
V_{DDQ}	Supply	**DQ Power Supply** : 1.8V +/- 0.1V
V_{SSQ}	Supply	**DQ Ground**
V_{DDL}	Supply	**DLL Power Supply** : 1.8V +/- 0.1V
V_{SSDL}	Supply	**DLL Ground**
V_{DD}	Supply	**Power Supply** : 1.8V +/- 0.1V
V_{SS}	Supply	**Ground**
V_{REF}	Supply	**Reference voltage**.

2. Functional Description

2.1 Simplified State Diagram



Note: Use caution with this diagram. It is indented to provide a floorplan of the possible state transitions and the commands to control them, not all details. In particular situations involving more than one bank, enabling/disabling on-die termination, Power Down enty/exit - among other things - are not captured in full detail.

2.2 Basic Function & Operation of DDR2 SDRAM

Read and write accesses to the DDR2 SDRAM are burst oriented; accesses start at a selected location and continue for a burst length of four or eight in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the active command are used to select the bank and row to be accessed (BA0-BA1 select the bank; A0-A12 select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst access and to determine if the auto precharge command is to be issued.

Prior to normal operation, the DDR2 SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

2.2.1 Power up and Initialization

DDR2 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

Power-up and Initialization Sequence

The following sequence is required for POWER UP and Initialization.

1. Apply power and attempt to maintain CKE below 0.2*VDDQ and ODT[*1] at a low state (all other inputs may be undefined.)

   - VDD, VDDL and VDDQ are driven from a single power converter output, AND
   - VTT is limited to 0.95 V max, AND
   - Vref tracks VDDQ/2.

   or

   - Apply VDD before or at the same time as VDDL.
   - Apply VDDL before or at the same time as VDDQ.
   - Apply VDDQ before or at the same time as VTT & Vref.

   at least one of these two sets of conditions must be met.

2. Start clock and maintain stable condition.
3. For the minimum of 200 us after stable power and clock(CK, $\overline{CK}$), then apply NOP or deselect & take CKE high.
4. Wait minimum of 400ns then issue precharge all command. NOP or deselect applied during 400ns period.
5. Issue EMRS(2) command. (To issue EMRS(2) command, provide “Low” to BA0, “High” to BA1.)[*2]
6. Issue EMRS(3) command. (To issue EMRS(3) command, provide “High” to BA0 and BA1.)[*2]
7. Issue EMRS to enable DLL. (To issue "DLL Enable" command, provide "Low" to A0, "High" to BA0 and "Low" to BA1.)
8. Issue a Mode Register Set command for “DLL reset”.
   (To issue DLL reset command, provide "High" to A8 and "Low" to BA0-1.)
9. Issue precharge all command.
10. Issue 2 or more auto-refresh commands.
11. Issue a mode register set command with low to A8 to initialize device operation. (i.e. to program operating parameters without resetting the DLL.)
12. At least 200 clocks after step 8, execute OCD Calibration (Off Chip Driver impedance adjustment). If OCD calibration is not used, EMRS OCD Default command (A9=A8= A7=1) followed by EMRS OCD Calibration Mode Exit command (A9=A8=A7=0) must be issued with other operating parameters of

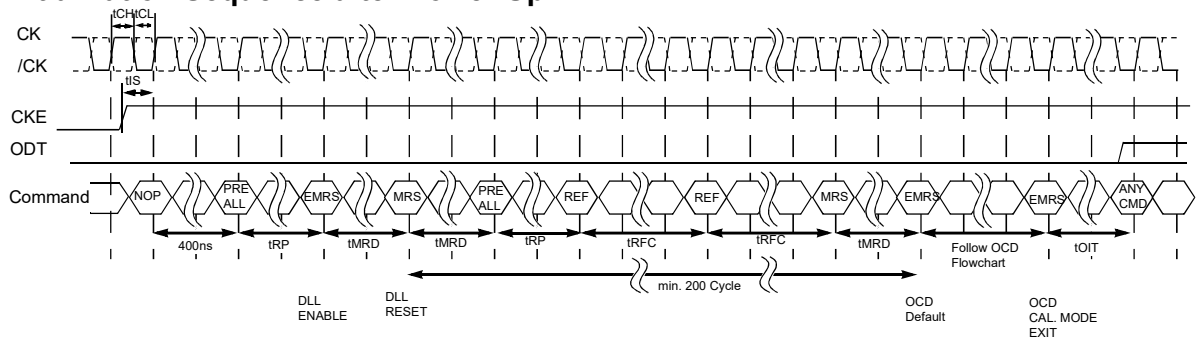
EMRS.

13. The DDR2 SDRAM is now ready for nomal operation.

*1) To guarantee ODT off, VREF must be valid and a low level must be applied to the ODT pin.

*2) Sequence 5 and 6 may be performed between 8 and 9.

Initialization Sequence after Power Up



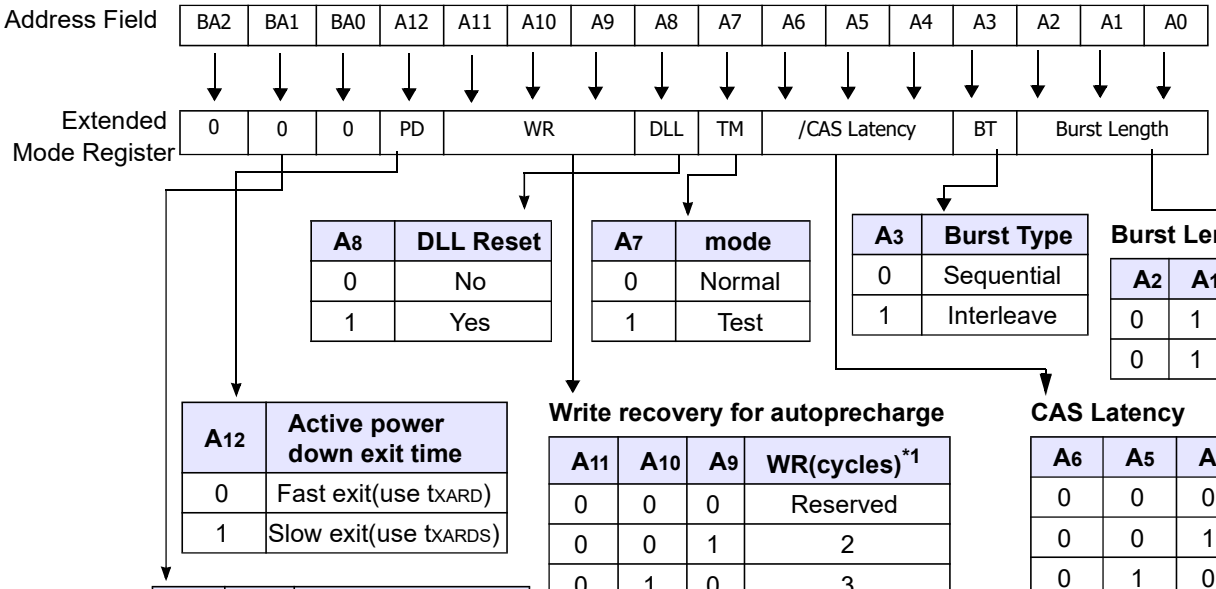
2.2.2 Programming the Mode and Extended Mode Registers

For application flexibility, burst length, burst type, $\overline{\text{CAS}}$ latency, DLL reset function, write recovery time(tWR) are user defined variables and must be programmed with a Mode Register Set (MRS) command. Additionally, DLL disable function, driver impedance, additive CAS latency, ODT(On Die Termination), single-ended strobe, and OCD(off chip driver impedance adjustment) are also user defined variables and must be programmed with an Extended Mode Register Set (EMRS) command. Contents of the Mode Register(MR) or Extended Mode Registers(EMR(#)) can be altered by re-executing the MRS and EMRS Commands. If the user chooses to modify only a subset of the MRS or EMRS variables, all variables must be redefined when the MRS or EMRS commands are issued.

MRS, EMRS and Reset DLL do not affect array contents, which means reinitialization including those can be executed any time after power-up without affecting array contents.

2.2.2.1 DDR2 SDRAM Mode Register Set (MRS)

The mode register stores the data for controlling the various operating modes of DDR2 SDRAM. It controls CAS latency, burst length, burst sequence, test mode, DLL reset, tWR and various vendor specific options to make DDR2 SDRAM useful for various applications. The default value of the mode register is not defined, therefore the mode register must be written after power-up for proper operation. The mode register is written by asserting low on CS, RAS, CAS, WE, BA0 and BA1, while controlling the state of address pins A0 ~ A12. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the mode register. The mode register set command cycle time (tMRD) is required to complete the write operation to the mode register. The mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. The mode register is divided into various fields depending on functionality. Burst length is defined by A0 ~ A2 with options of 4 and 8 bit burst lengths. The burst length decodes are compatible with DDR SDRAM. Burst address sequence type is defined by A3, CAS latency is defined by A4 ~ A6. The DDR2 doesn't support half clock latency mode. A7 is used for test mode. A8 is used for DLL reset. A7 must be set to low for normal MRS operation. Write recovery time tWR is defined by A9 ~ A11. Refer to the table for specific codes.



A8	DLL Reset
0	No
1	Yes

A7	mode
0	Normal
1	Test

A3	Burst Type
0	Sequential
1	Interleave

Burst Length

A2	A1	A0	BL
0	1	0	4
0	1	1	8

A12	Active power down exit time
0	Fast exit(use t_{XARD})
1	Slow exit(use t_{XARDS})

Write recovery for autoprecharge

A11	A10	A9	WR(cycles)*1
0	0	0	Reserved
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	Reserved

CAS Latency

A6	A5	A4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

BA1	BA0	MRS mode
0	0	MRS
0	1	EMRS(1)
1	0	EMRS(2)
1	1	EMRS(3): Reserved

MRS Default setting

Active Power donw exit	WR	/CAS Latency	BT	Burst Length
Fast Exit	WR=4	CL=4	Seq.	BL=4

*1: WR(write recovery for autoprecharge) min is determined by tCK max and WR max is determined by tCK min. WR in clock cycles is calculated by dividing tWR (in ns) by tCK (in ns) and rounding up to the next integer (WR[cycles] = tWR(ns)/tCK(ns)). The mode register must be programmed to this value. This is also used with tRP to determine tDAL.

2.2.2.2 DDR2 SDRAM Extended Mode Register Set

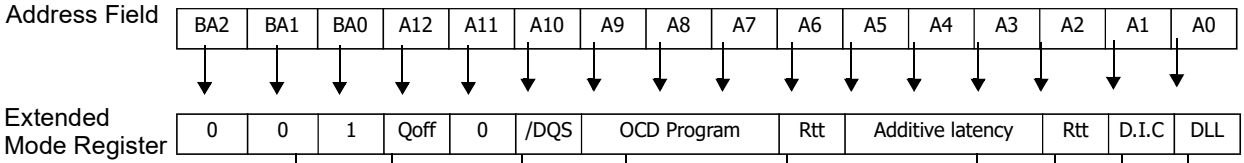
EMRS(1)

The extended mode register(1) stores the data for enabling or disabling the DLL, output driver strength, additive latency, ODT, $\overline{DQS}$ disable, OCD program. The default value of the extended mode register(1) is not defined, therefore the extended mode register(1) must be written after power-up for proper operation. The extended mode register(1) is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, high on BA0 and low on BA1, while controlling the states of address pins A0 ~ A12. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register(1). The mode register set command cycle time (tMRD) must be satisfied to complete the write operation to the extended mode register(1). Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. A0 is used for DLL enable or disable. A1 is used for enabling a half strength output driver. A3~A5 determines the additive latency, A7~A9 are used for OCD control, A10 is used for $\overline{DQS}$ disable. A2 and A6 are used for ODT setting.

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. The DLL is automatically disabled when entering self refresh operation and is automatically re-enabled upon exit of self refresh operation. Any time the DLL is enabled (and subsequently reset), 200 clock cycles must occur before a Read command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tAC or tDQSCK parameters.

EMRS(1) Programming



BA1	BA0	MRS mode
0	0	MRS
0	1	EMRS(1)
1	0	EMRS(2)
1	1	EMRS(3): Reserved

A6	A2	R_{tt} (NOMINAL)
0	0	ODT Disabled
0	1	75 ohm
1	0	150 ohm
1	1	50 ohm

A_0	DLL Enable
0	Enable
1	Disable

A_5	A_4	A_3	Additive Latency
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	Reserved

A9	A8	A7	OCD Calibration Program
0	0	0	OCD Calibration mode exit; maintain setting
0	0	1	Drive(1)
0	1	0	Drive(0)
1	0	0	Adjust mode[a]
1	1	1	OCD Calibration default [b]

a: When Adjust mode is issued, AL from previously set value must be applied.
b: After setting to default, OCD mode needs to be exited by setting A9-A7 to 000. Refer to the following 2.2.2.3 section for detailed information

A_{12}	Qoff
0	Output buffer enabled
1	Output buffer disabled

A10 (/DQS Enable)	Strobe Function Matrix	
	DQS	/DQS
0(Enable)	DQS	/DQS
1(Disable)	DQS	Hi-z

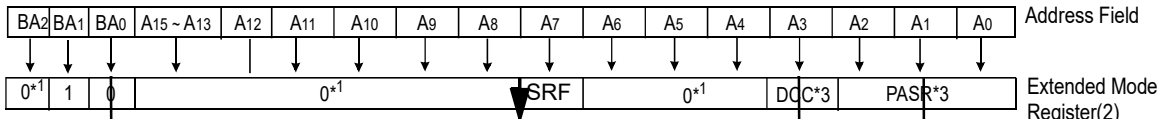
A10	$\overline{DQS}$
0	Enable
1	Disable

A1	Output Driver Impedence Control	Driver Size
0	Normal	100%
1	Weak	60%

EMR(2)

The extended mode register(2) controls refresh related features. The default value of the extended mode register(2) is not defined, therefore the extended mode register(2) must be programmed during initialization for proper operation. The extended mode register(2) is written by asserting LOW on /CS,/RAS,/CAS,/WE, HIGH on BA1 and LOW on BA0, while controling the states of address pins A0~A15. The DDR2 SDRAM should be in all bank precharge with CKE already HIGH prior to writing into the extended mode register(2). The mode register set command cycle time(tMRD) must be satisfied to complete the write operation to the extended mode register(2). Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state.

EMR(2) Programming:



A7	High Temp Self-refresh Rate Enable
0	Disable
1	Enable(Optional)*2

BA1	BA0	MR mode
0	0	MR
0	1	EMR(1)
1	0	EMR(2)
1	1	EMR(3):Reserved

A3	DCC Enable(Optional)*4
0	Disable
1	Enable

A2	A1	A0	Partial Array Self Refresh for 8 banks	Partial Array Self Refresh for 4 banks
0	0	0	Full Array	Full Array
0	0	1	Half Array (BA[2:0]=000,001,010&011)	Half Array (BA[1:0]=00&01)
0	1	0	Quarter Array (BA[2:0]=000&001)	Quarter Array (BA[1:0]=00)
0	1	1	1/8th Array (BA[2:0]=000)	Not Defined
1	0	0	3/4 Array (BA[2:0]=010,011,100,101,110&111)	3/4 Array (BA[1:0]=01,10&11)
1	0	1	Half Array (BA[2:0]=100,101,110&111)	Half Array (BA[1:0]=10&11)
1	1	0	Quarter Array (BA[2:0]=110&111)	Quarter Array (BA[1:0]=11)
1	1	1	1/8th Array (BA[2:0]=111)	Not Defined

*1 : The rest bits in EMR(2) are reserved for future use and all bits except A7, BA0 and BA1 must be programmed to 0 when setting the mode register during initialization.

*2 : Currently the periodic Self-Refresh interval is hard coded whithin the DRAM to a specific value. EMR(2) bit A7 is a migration plan to support higher Self-Refresh entry. However, since this Self-Refresh control function is an option and to be phased-in by manufacturer individually, checking on the DRAM parts for function availablity is necessary. For more details, please refer to “Operating Temperature Condition” section at “Chapter 5. AC & DC operation conditions”.

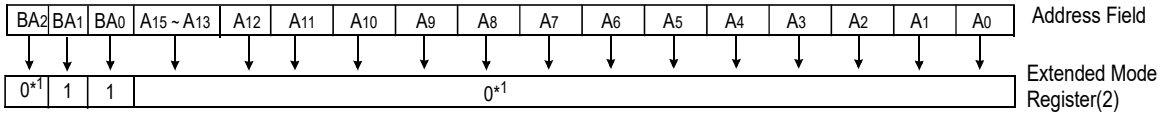
*3 Optional in DDR2 SDRAM. If PASR (Partial Array Self Refresh) is enabled, data located in areas of the array beyond the specified address range will be lost if self refresh is entered. Data integrity will be maintained if tREF conditions are met and no Self Refresh command is issued. If the PASR feature is not supported, EMR(2)[A0-A2] must be set to 000 when programming EMR(2).

*4 Optional in DDR2 SDRAM. JEDEC standard DDR2 SDRAM may or may not have DCC (Duty Cycle Corrector) implemented, and in some of the DRAMs implementing DCC, user may be given the controllability of DCC thru EMR(2)[A3] bit. JEDEC standard DDR2 SDRAM users can look at manufacturer's data sheet to check if the DRAM part supports DCC controllability. If Optional DCC Controllability is supported, user may enable or disable the DCC by programming EMR(2)[A3] accordingly. If the controllability feature is not supported, EMR(2)[A3] must be set to 0 when programming EMR(2).

EMR(3)

No function is defined in extended mode register(3). The default value of the extended mode register(3) is not defined, therefore the extended mode register(3) must be programmed during initialization for proper operation.

EMR(3) Programming:

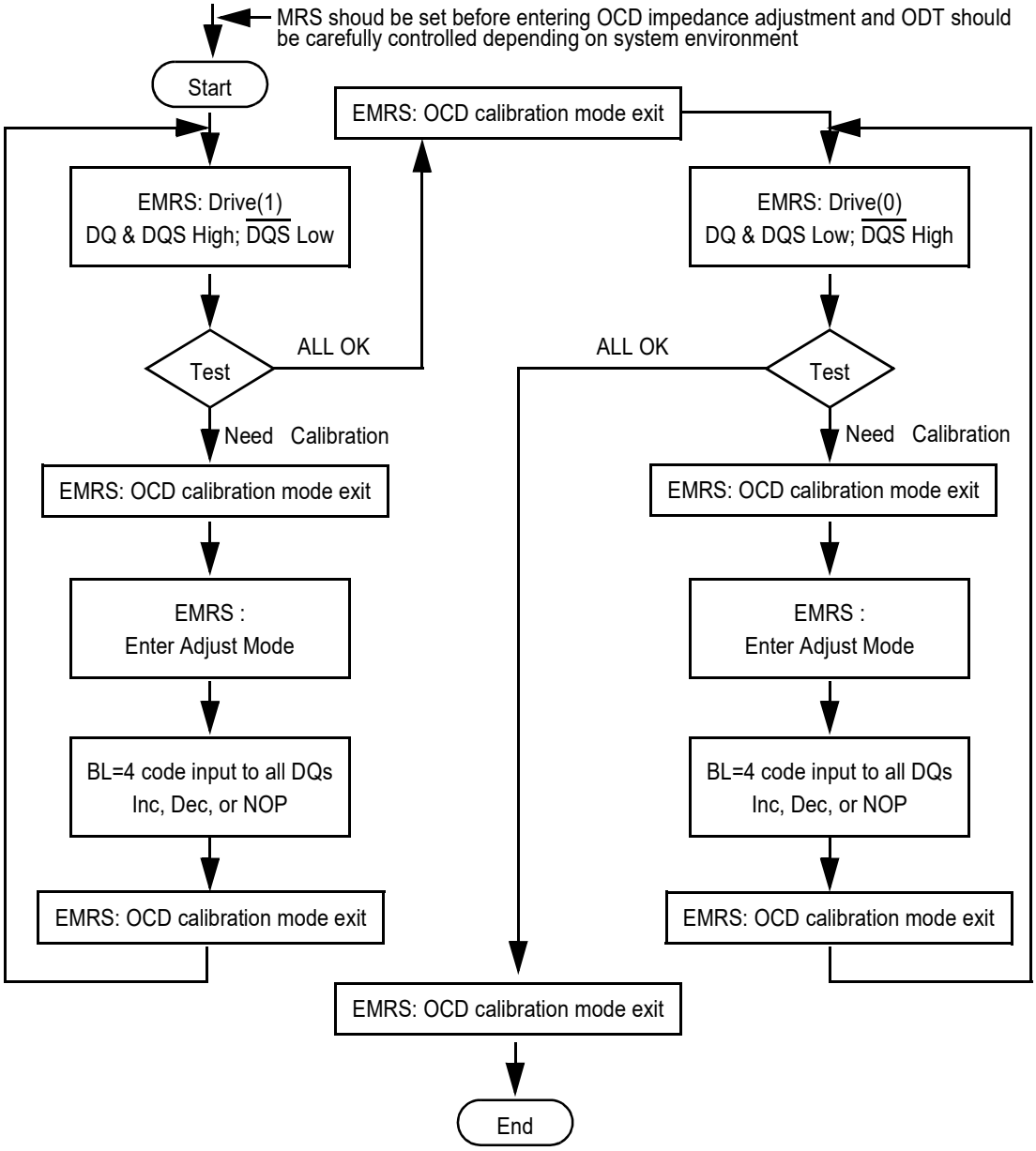


*1 :All bits in EMR(3) except BA0 and BA1 are reserved for future use and must be programmed to 0 when setting the mode register during initialization.

Figure 6. EMR(3) programming

2.2.2.3 Off-Chip Driver (OCD) Impedance Adjustment

DDR2 SDRAM supports driver calibration feature and the flow chart below is an example of sequence. Every calibration mode command should be followed by "OCD calibration mode exit" before any other command being issued. MRS should be set before entering OCD impedance adjustment and ODT (On Die Termination) should be carefully controlled depending on system environment.



Extended Mode Register Set for OCD impedance adjustment

OCD impedance adjustment can be done using the following EMRS mode. In drive mode all outputs are driven out by DDR2 SDRAM. In Drive(1) mode, all DQ, DQS signals are driven high and all $\overline{DQS}$ signals are driven low. In drive(0) mode, all DQ, DQS signals are driven low and all $\overline{DQS}$ signals are driven high. In adjust mode, BL = 4 of operation code data must be used. In case of OCD calibration default, output driver characteristics have a nominal impedance value of 18 ohms during nominal temperature and voltage conditions. Output driver characteristics for OCD calibration default are specified in Table x. OCD applies only to normal full strength output drive setting defined by EMRS(1) and if half strength is set, OCD default output driver

characteristics are not applicable. When OCD calibration adjust mode is used, OCD default output driver characteristics are not applicable. After OCD calibration is completed or driver strength is set to default, subsequent EMRS commands not intended to adjust OCD characteristics must specify A9-A7 as '000' in order to maintain the default or calibrated value.

Off- Chip-Driver program

A9	A8	A7	Operation
0	0	0	OCD calibration mode exit
0	0	1	Drive(1) DQ, DQS high and $\overline{DQS}$ low
0	1	0	Drive(0) DQ, DQS low and $\overline{DQS}$ high
1	0	0	Adjust mode
1	1	1	OCD calibration default

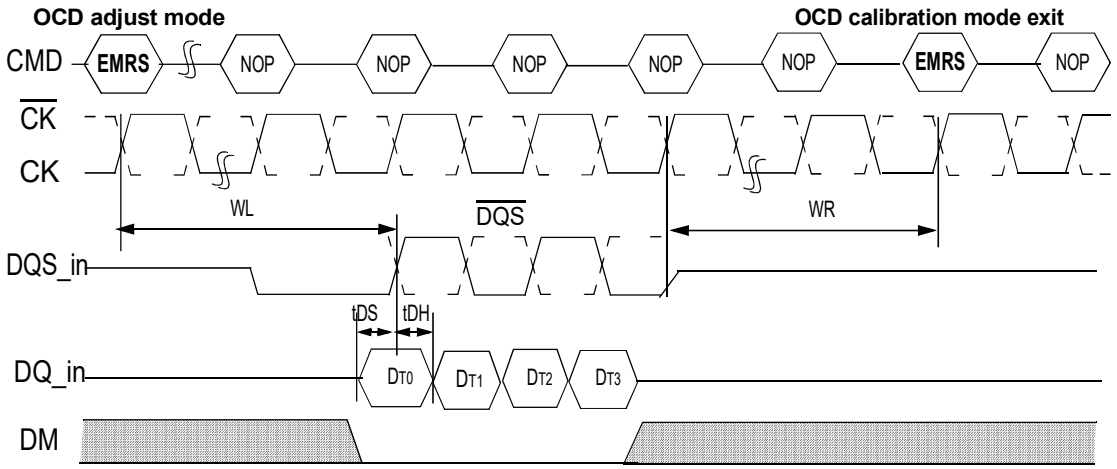
OCD impedance adjust

To adjust output driver impedance, controllers must issue the ADJUST EMRS command along with a 4bit burst code to DDR2 SDRAM as in table X. For this operation, Burst Length has to be set to BL = 4 via MRS command before activating OCD and controllers must drive this burst code to all DQs at the same time. DT0 in table X means all DQ bits at bit time 0, DT1 at bit time 1, and so forth. The driver output impedance is adjusted for all DDR2 SDRAM DQs simultaneously and after OCD calibration, all DQs of a given DDR2 SDRAM will be adjusted to the same driver strength setting. The maximum step count for adjustment is 16 and when the limit is reached, further increment or decrement code has no effect. The default setting may be any step within the 16 step range. When Adjust mode command is issued, AL from previously set value must be applied

Table X : Off- Chip-Driver Program

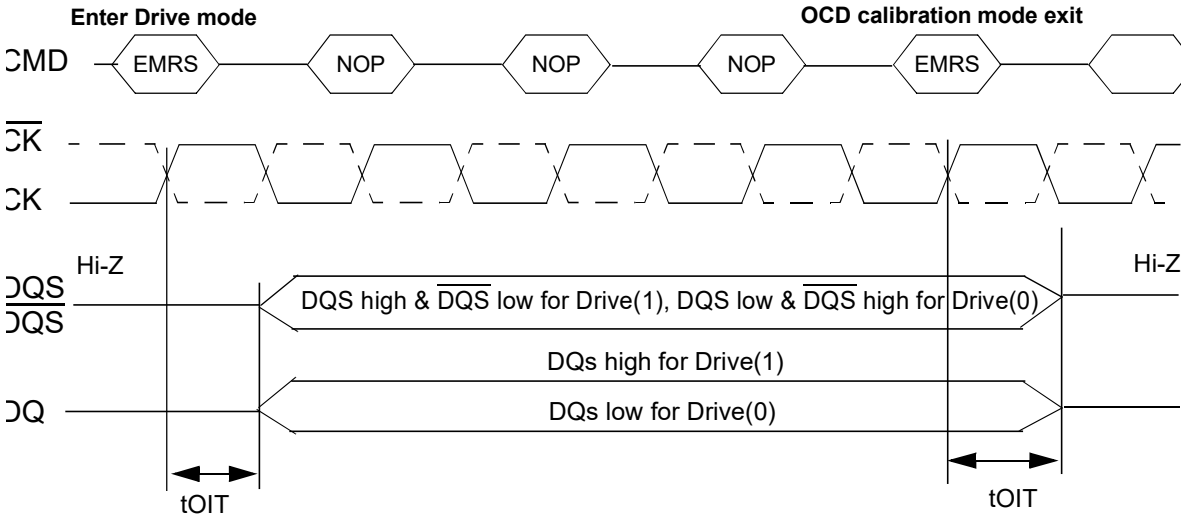
4bit burst code inputs to all DQs				Operation	
D_{T0}	D_{T1}	D_{T2}	D_{T3}	Pull-up driver strength	Pull-down driver strength
0	0	0	0	NOP (No operation)	NOP (No operation)
0	0	0	1	Increase by 1 step	NOP
0	0	1	0	Decrease by 1 step	NOP
0	1	0	0	NOP	Increase by 1 step
1	0	0	0	NOP	Decrease by 1 step
0	1	0	1	Increase by 1 step	Increase by 1 step
0	1	1	0	Decrease by 1 step	Increase by 1 step
1	0	0	1	Increase by 1 step	Decrease by 1 step
1	0	1	0	Decrease by 1 step	Decrease by 1 step
Other Combinations				Reserved	

For proper operation of adjust mode, WL = RL - 1 = AL + CL - 1 clocks and tDS/tDH should be met as the following timing diagram. For input data pattern for adjustment, DT0 - DT3 is a fixed order and "not affected by
MRS addressing mode (ie. sequential or interleave).



Drive Mode

Drive mode, both Drive(1) and Drive(0), is used for controllers to measure DDR2 SDRAM Driver impedance. In this mode, all outputs are driven out tOIT after “enter drive mode” command and all output drivers are turned-off tOIT after “OCD calibration mode exit” command as the following timing diagram.

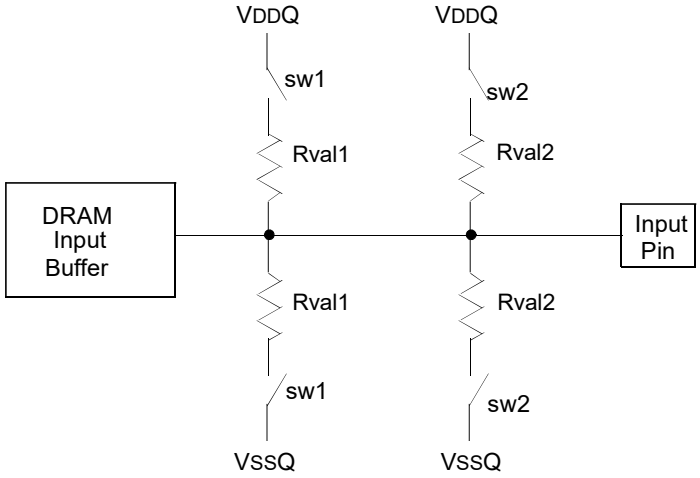


2.2.2.4 ODT (On Die Termination)

On Die Termination (ODT) is a feature that allows a DRAM to turn on/off termination resistance for DQ, UDQS/$\overline{\text{UDQS}}$, LDQS/$\overline{\text{LDQS}}$, UDM, and LDM signal via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

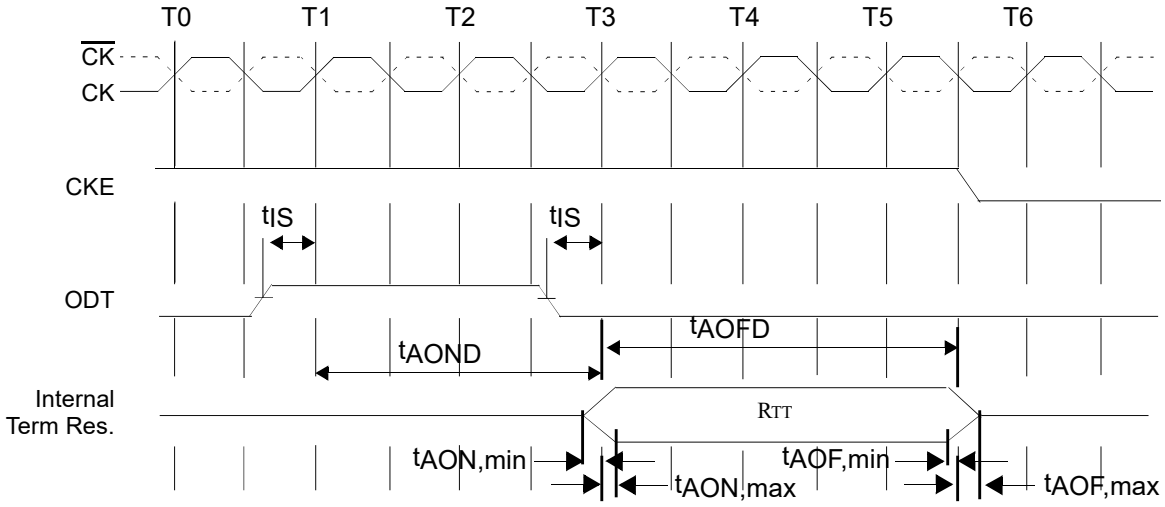
The ODT function is supported for ACTIVE and STANDBY modes. ODT is turned off and not supported in SELF REFRESH mode.

FUNCTIONAL REPRESENTATION OF ODT

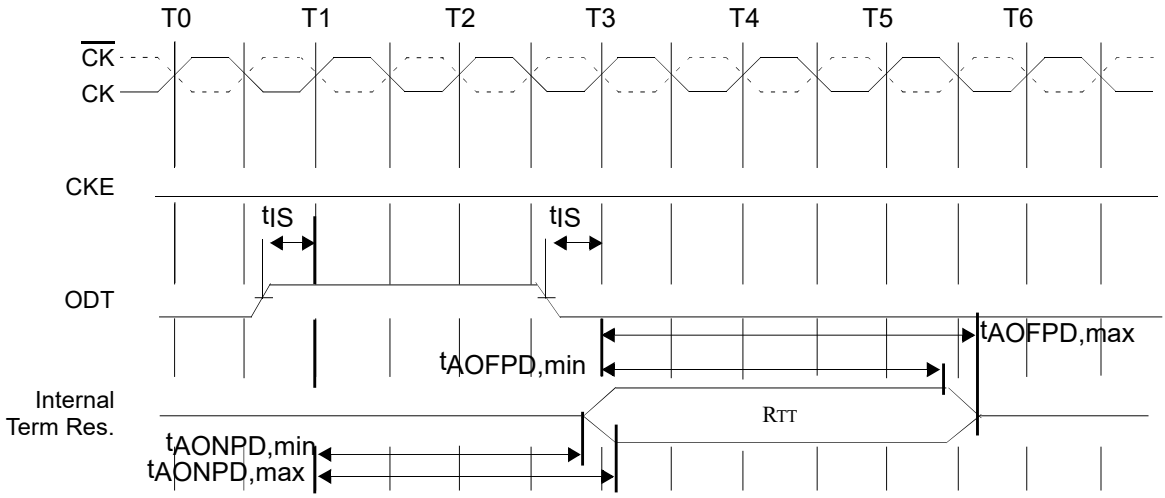


Switch sw1 or sw2 is enabled by ODT pin.
Selection between sw1 or sw2 is determined by "Rtt (nominal)" in EMRS
Termination included on all DQs, DM, DQS, $\overline{\text{DQS}}$ pins.
Target Rtt (ohm) = (Rval1) / 2 or (Rval2) / 2

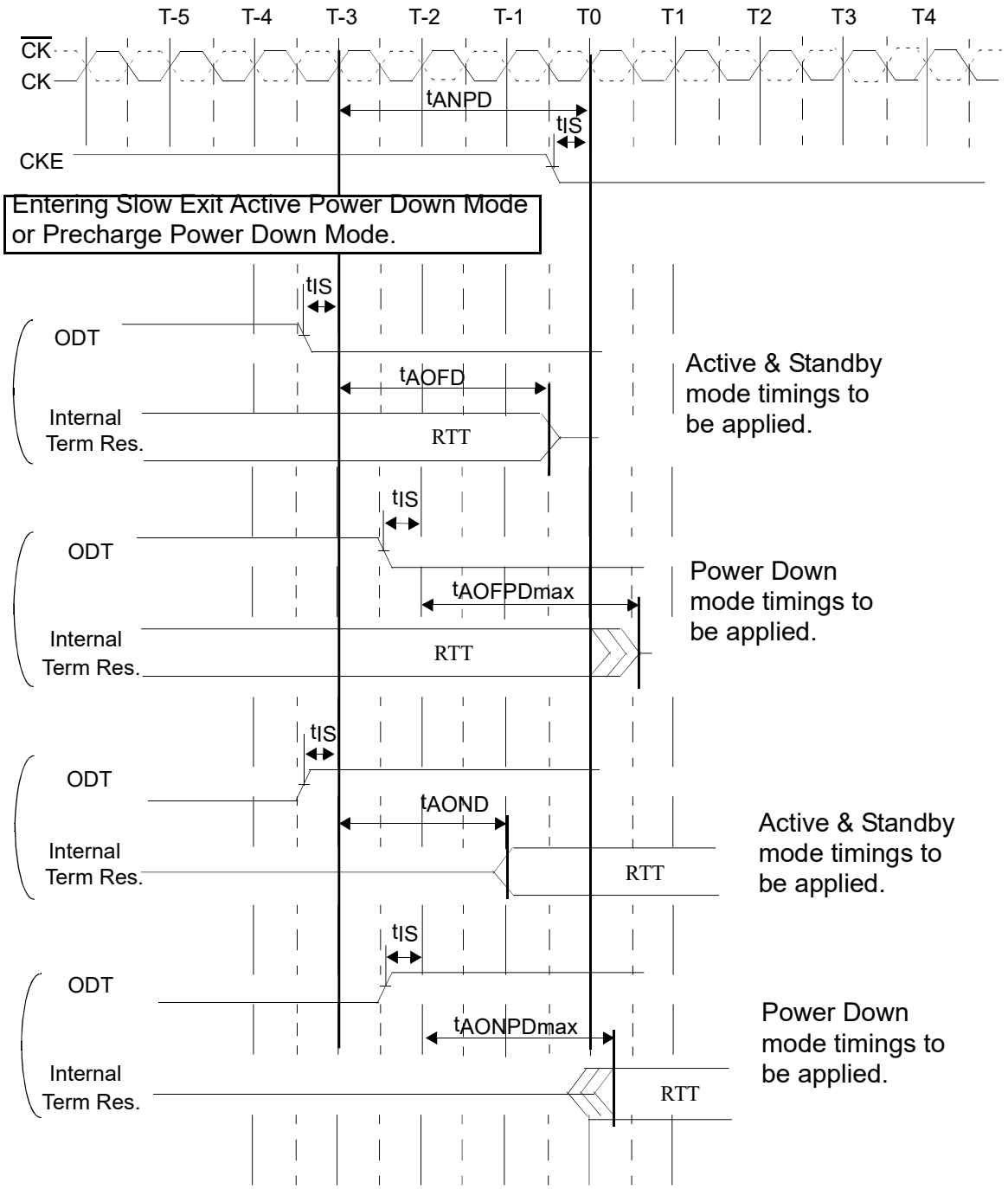
ODT timing for active/standby mode



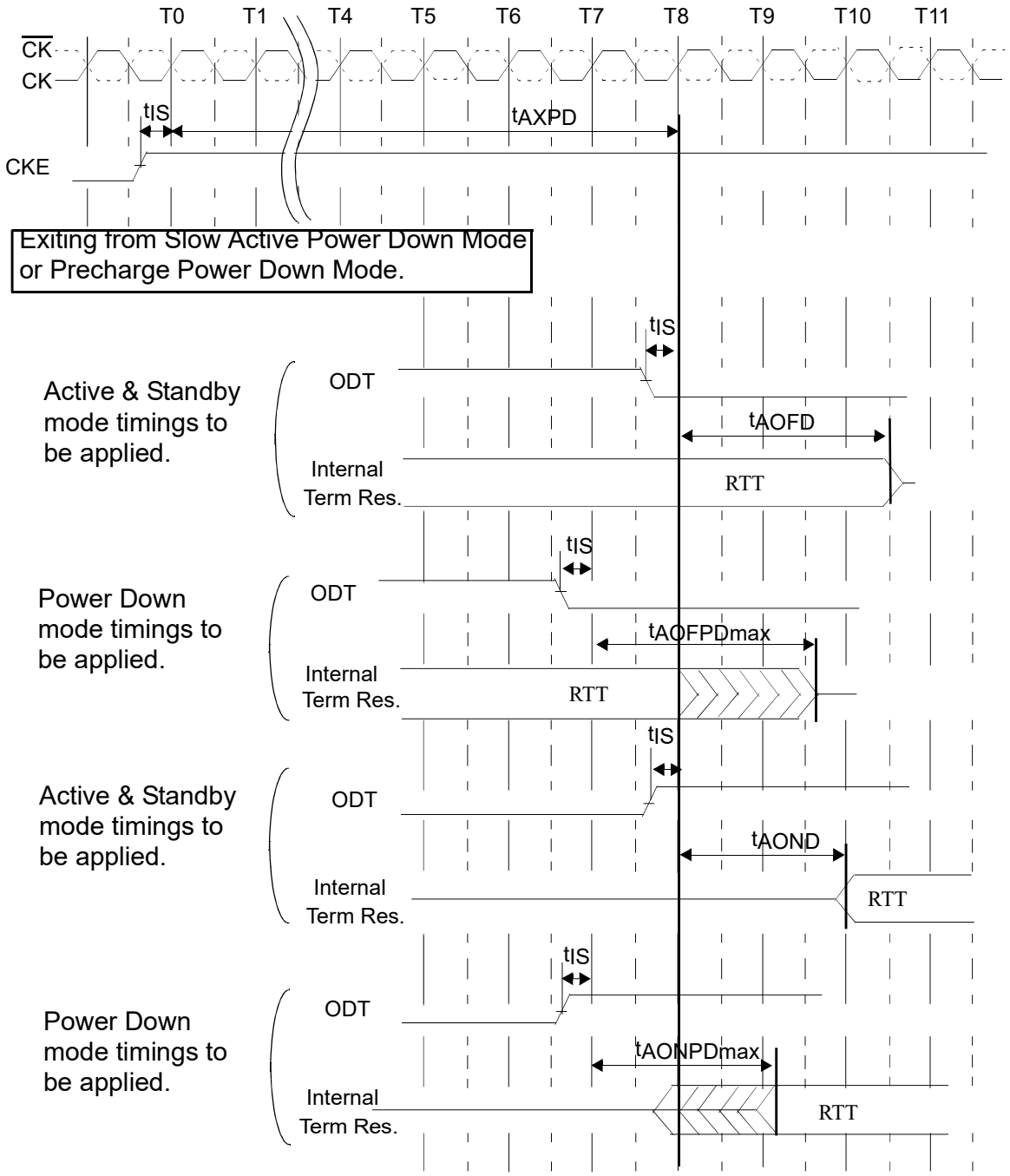
ODT timing for powerdown mode



ODT timing mode switch at entering power down mode



ODT timing mode switch at exiting power down mode



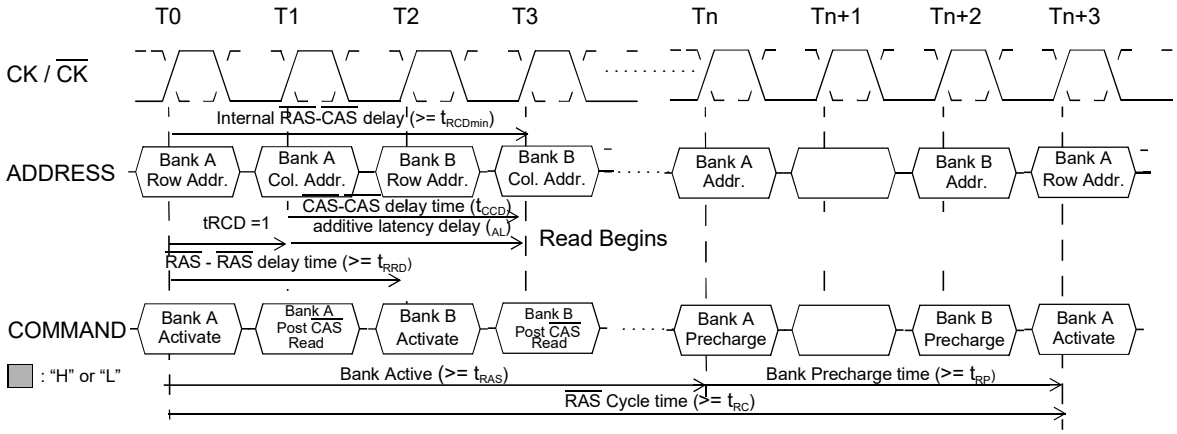
2.3 Bank Activate Command

The Bank Activate command is issued by holding $\overline{CAS}$ and $\overline{WE}$ HIGH with $\overline{CS}$ and $\overline{RAS}$ LOW at the rising edge of the clock. The bank addresses BA0 ~ BA2 are used to select the desired bank. The row address A0 through A15 is used to determine which row to activate in the selected bank. The Bank Activate command must be applied before any Read or Write operation can be executed. Immediately after the bank active command, the DDR2 SDRAM can accept a read or write command on the following clock cycle. If a R/W command is issued to a bank that has not satisfied the tRCDmin specification, then additive latency must be programmed into the device to delay when the R/W command is internally issued to the device. The additive latency value must be chosen to assure tRCDmin is satisfied. Additive latencies of 0, 1, 2, 3 and 4 are supported. Once a bank has been activated it must be precharged before another Bank Activate command can be applied to the same bank. The bank active and precharge times are defined as tRAS and tRP, respectively. The minimum time interval between successive Bank Activate commands to the same bank is determined by the RAS cycle time of the device (t_{RC}). The minimum time interval between Bank Activate commands is t_{RRD}.

In order to ensure that 8 bank devices do not exceed the instantaneous current supplying capability of 4 bank devices, certain restrictions on operation of the 8 bank devices must be observed. There are two rules. One for restricting the number of sequential ACT commands that can be issued and another for allowing more time for RAS precharge for a Precharge All command. The rules are as follows:

* 8 bank device Sequential Bank Activation Restriction: No more than 4 banks may be activated in a rolling tFAW window. Converting to clocks is done by dividing tFAW[ns] by tCK[ns] or tCK(avg)[ns], depending on the speed bin, and rounding up to next integer value. As an example of the rolling window, if (tFAW/tCK) or (tFAW/tCK(avg) rounds up to 10 clocks, and an activate command is issued in clock N, no more than three further activate commands may be issued at or betwen clock N+1 through N+9.

* 8 bank device Precharge All Allowance : tRP for a Precharge All command for an 8 Bank device will equal to tRP+1*tCK or tnRP + 1*nCK, depending on the speed bin, where tnRP=tRP/tCK(avg) rounded up to the next interger, where tRP is the value for a single bank pre-charge.



Bank Activate Command Cycle: tRCD = 3, AL = 2, tRP = 3, tRRD = 2, tCCD = 2

2.4 Read and Write Command

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting $\overline{RAS}$ high, $\overline{CS}$ and $\overline{CAS}$ low at the clock's rising edge. $\overline{WE}$ must also be defined at this time to determine whether the access cycle is a read operation ($\overline{WE}$ high) or a write operation ($\overline{WE}$ low).

The DDR2 SDRAM provides a fast column access operation. A single Read or Write Command will initiate a serial read or write operation on successive clock cycles. The boundary of the burst cycle is strictly restricted to specific segments of the page length. For example, the 32Mbit x 4 I/O x 4 Bank chip has a page length of 2048 bits (defined by CA0-CA9, CA11). The page length of 2048 is divided into 512 or 256 uniquely addressable boundary segments depending on burst length, 512 for 4 bit burst, 256 for 8 bit burst respectively. A 4-bit or 8 bit burst operation will occur entirely within one of the 512 or 256 groups beginning with the column address supplied to the device during the Read or Write Command (CA0-CA9, CA11). The second, third and fourth access will also occur within this group segment, however, the burst order is a function of the starting address, and the burst sequence.

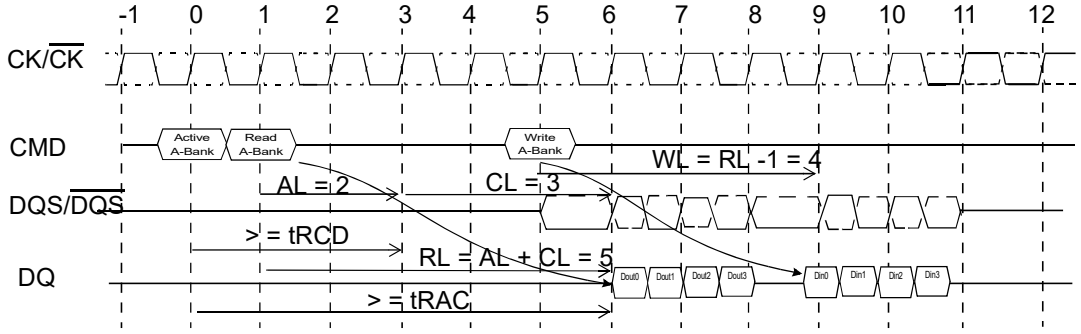
A new burst access must not interrupt the previous 4 bit burst operation in case of BL = 4 setting. However, in case of BL = 8 setting, two cases of interrupt by a new burst access are allowed, one reads interrupted by a read, the other writes interrupted by a write with 4 bit burst boundry respectively. The minimum $\overline{CAS}$ to $\overline{CAS}$ delay is defined by tCCD, and is a minimum of 2 clocks for read or write cycles.

2.4.1 Posted CAS

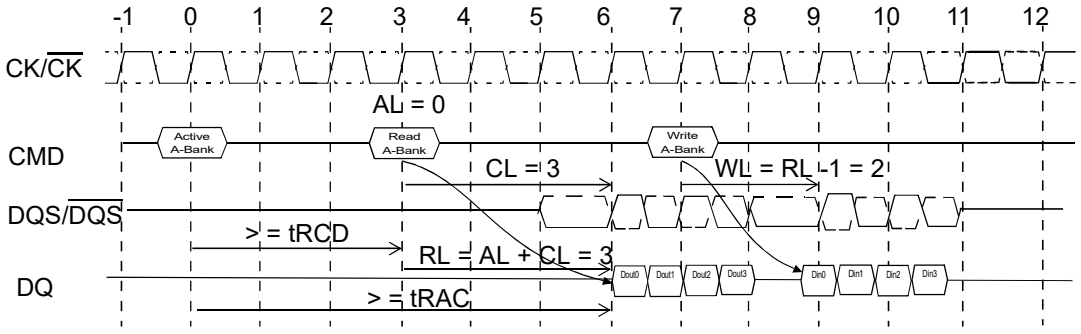
Posted CAS operation is supported to make command and data bus efficient for sustainable bandwidths in DDR2 SDRAM. In this operation, the DDR2 SDRAM allows a CAS read or write command to be issued immediately after the RAS bank activate command (or any time during the RAS-CAS-delay time, tRCD, period). The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of AL and the CAS latency (CL). Therefore if a user chooses to issue a R/W command before the tRCDmin, then AL (greater than 0) must be written into the EMRS(1). The Write Latency (WL) is always defined as RL - 1 (read latency -1) where read latency is defined as the sum of additive latency plus CAS latency (RL=AL+CL). Read or Write operations using AL allow seamless bursts (refer to seamless operation timing diagram examples in Read burst and Wirte burst section)

Examples of posted CAS operation

Example 1 Read followed by a write to the same bank
[AL = 2 and CL = 3, RL = (AL + CL) = 5, WL = (RL - 1) = 4, BL = 4]



Example 2 Read followed by a write to the same bank
[AL = 0 and CL = 3, RL = (AL + CL) = 3, WL = (RL - 1) = 2, BL = 4]



2.4.2 Burst Mode Operation

Burst mode operation is used to provide a constant flow of data to memory locations (write cycle), or from memory locations (read cycle). The parameters that define how the burst mode will operate are burst sequence and burst length. DDR2 SDRAM supports 4 bit burst and 8 bit burst modes only. For 8 bit burst mode, full interleave address ordering is supported, however, sequential address ordering is nibble based for ease of implementation. The burst type, either sequential or interleaved, is programmable and defined by the address bit 3 (A3) of the MRS, which is similar to the DDR SDRAM operation. Seamless burst read or write operations are supported. Unlike DDR devices, interruption of a burst read or write cycle during BL = 4 mode operation is prohibited. However in case of BL = 8 mode, interruption of a burst read or write operation is limited to two cases, reads interrupted by a read, or writes interrupted by a write. Therefore the Burst Stop command is not supported on DDR2 SDRAM devices.

Burst Length and Sequence

Burst Length	Starting Address (A2 A1 A0)	Sequential Addressing (decimal)	Interleave Addressing (decimal)
4	0 0 0	0, 1, 2, 3	0, 1, 2, 3
	0 0 1	1, 2, 3, 0	1, 0, 3, 2
	0 1 0	2, 3, 0, 1	2, 3, 0, 1
	0 1 1	3, 0, 1, 2	3, 2, 1, 0
8	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	0 0 1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6
	0 1 0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5
	0 1 1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4
	1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	1 0 1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2
	1 1 0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1
	1 1 1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0

Note: Page length is a function of I/O organization and column addressing

2.4.3 Burst Read Command

The Burst Read command is initiated by having $\overline{CS}$ and $\overline{CAS}$ low while holding $\overline{RAS}$ and $\overline{WE}$ high at the rising edge of the clock. The address inputs determine the starting column address for the burst. The delay from the start of the command to when the data from the first cell appears on the outputs is equal to the value of the read latency (RL). The data strobe output (DQS) is driven low 1 clock cycle before valid data (DQ) is driven onto the data bus. The first bit of the burst is synchronized with the rising edge of the data strobe (DQS). Each subsequent data-out appears on the DQ pin in phase with the DQS signal in a source synchronous manner. The RL is equal to an additive latency (AL) plus $\overline{CAS}$ latency (CL). The CL is defined by the Mode Register Set (MRS), similar to the existing SDR and DDR SDRAMs. The AL is defined by the Extended Mode Register Set (1)(EMRS(1)).

DDR2 SDRAM pin timings are specified for either single ended mode or differential mode depending on the setting of the EMRS(1) "Enable DQS" mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timings are measured is mode dependent. In single
ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at V_{REF}. In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, $\overline{DQS}$. This distinction in timing methods is guaranteed by design and characterization. Note that when differential data strobe mode is disabled via the EMRS, the complementary pin, $\overline{DQS}$, must be tied externally to VSS through a 20 ohm to 10 Kohm resistor to insure proper operation.

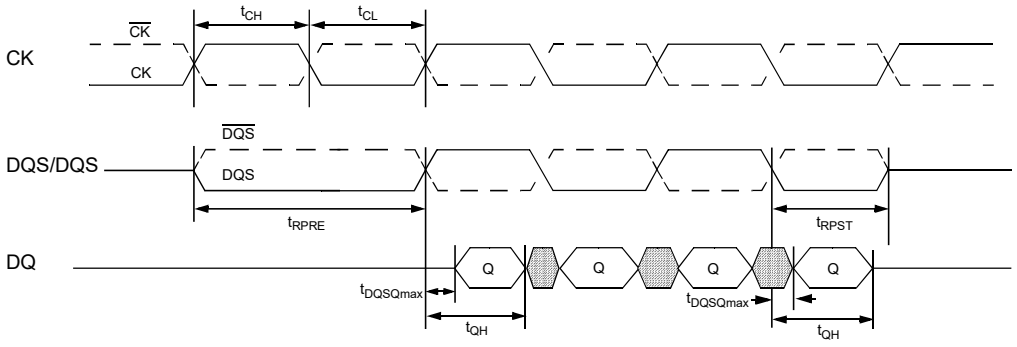
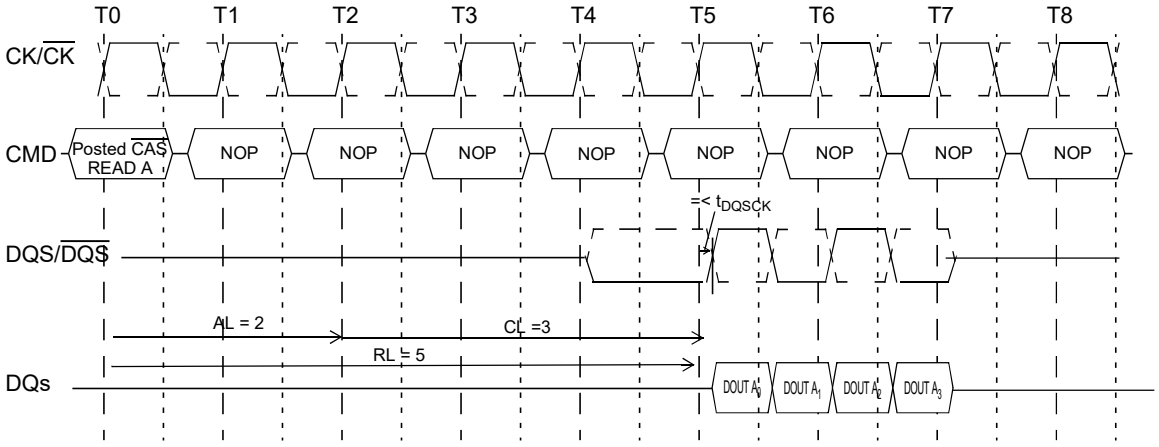
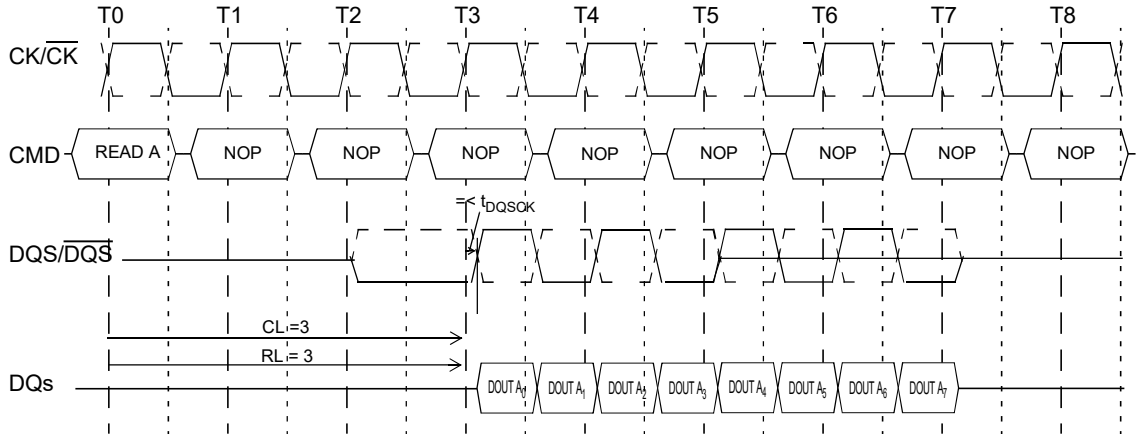


Figure YY-- Data output (read) timing

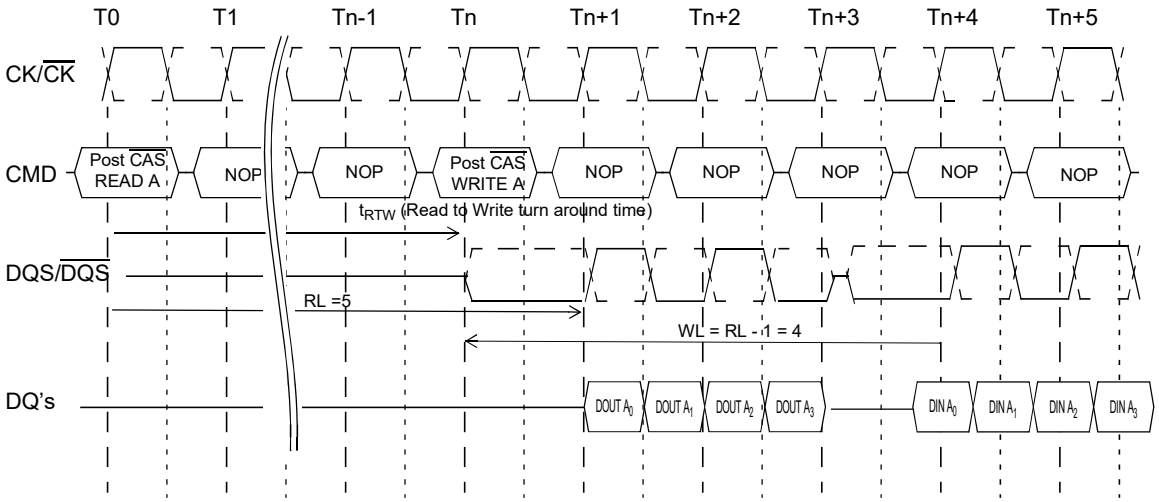
Burst Read Operation: RL = 5 (AL = 2, CL = 3, BL = 4)



Burst Read Operation: RL = 3 (AL = 0 and CL = 3, BL = 8)

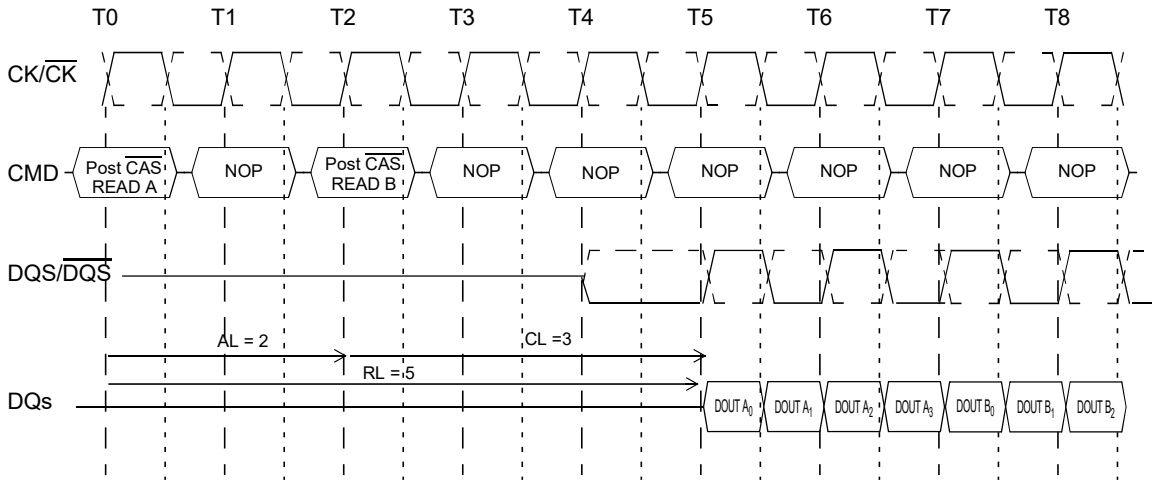


Burst Read followed by Burst Write: RL = 5, WL = (RL-1) = 4, BL = 4



The minimum time from the burst read command to the burst write command is defined by a read-to-write-turn-around-time, which is 4 clocks in case of BL = 4 operation, 6 clocks in case of BL = 8 operation.

Seamless Burst Read Operation: RL = 5, AL = 2, and CL = 3, BL = 4

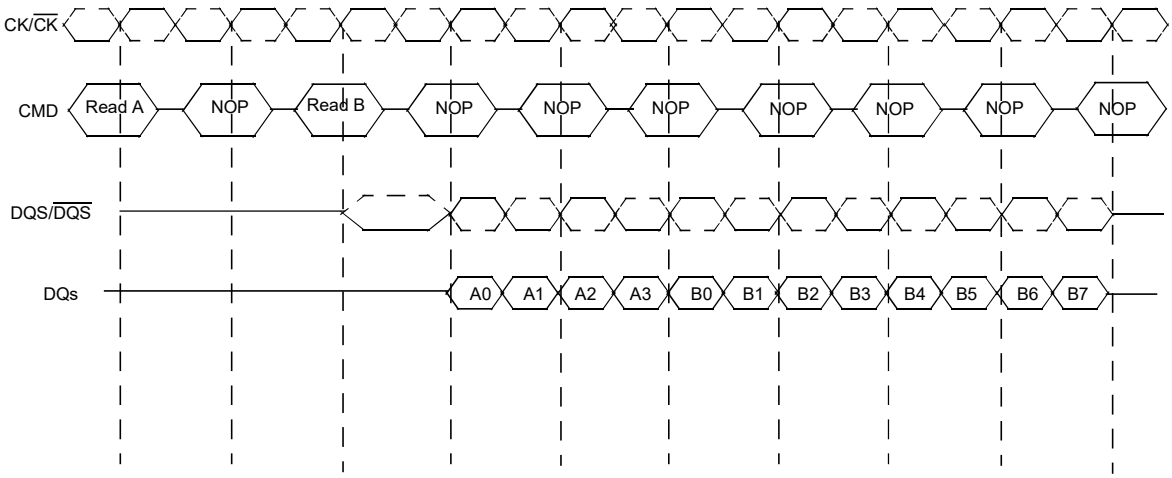


The seamless burst read operation is supported by enabling a read command at every other clock for BL = 4 operation, and every 4 clock for BL = 8 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

Reads interrupted by a read

Burst read can only be interrupted by another read with 4 bit burst boundary. Any other case of read interrupt is not allowed.

Read Burst Interrupt Timing Example: (CL=3, AL=0, RL=3, BL=8)

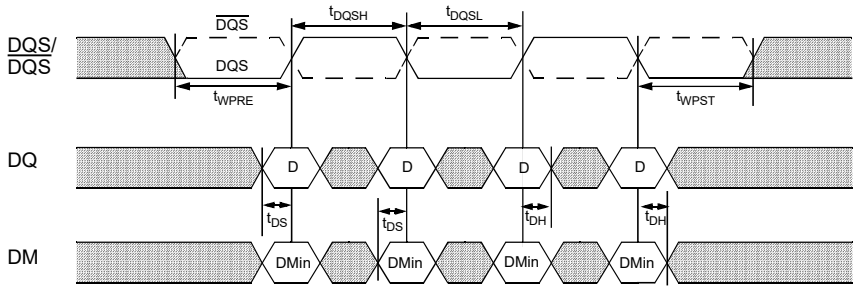


Note

1. Read burst interrupt function is only allowed on burst of 8. Burst interrupt of 4 is prohibited.
2. Read burst of 8 can only be interrupted by another Read command. Read burst interruption by Write command or Precharge command is prohibited.
3. Read burst interrupt must occur exactly two clocks after previous Read command. Any other Read burst interrupt timings are prohibited.
4. Read burst interruption is allowed to any bank inside DRAM.
5. Read burst with Auto Precharge enabled is not allowed to interrupt.
6. Read burst interruption is allowed by another Read with Auto Precharge command.
7. All command timings are referenced to burst length set in the mode register. They are not referenced to actual burst. For example, Minimum Read to Precharge timing is AL + BL/2 where BL is the burst length set in the mode register and not the actual burst (which is shorter because of interrupt).

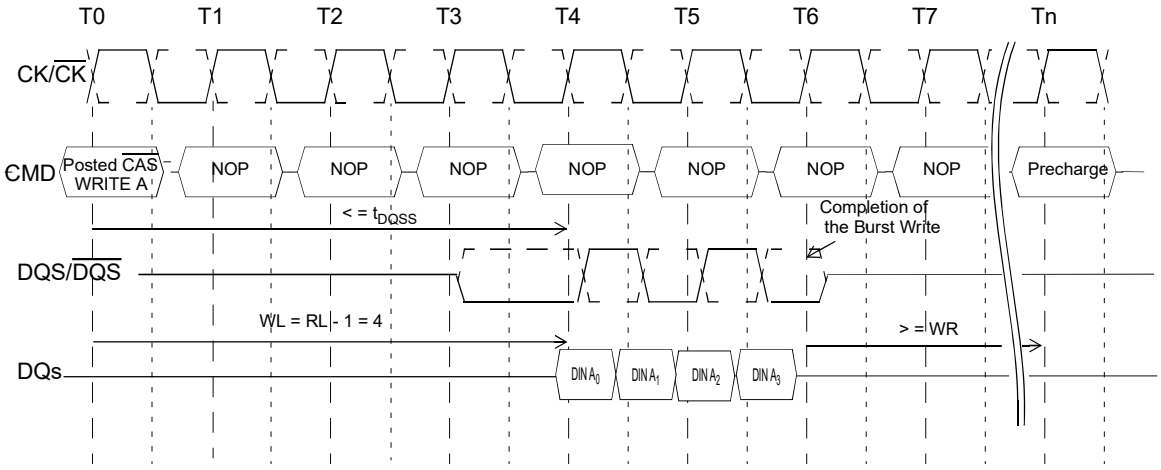
2.4.4 Burst Write Operation

The Burst Write command is initiated by having $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ low while holding $\overline{RAS}$ high at the rising edge of the clock. The address inputs determine the starting column address. Write latency (WL) is defined by a read latency (RL) minus one and is equal to (AL + CL -1). A data strobe signal (DQS) should be driven low (preamble) one clock prior to the WL. The first data bit of the burst cycle must be applied to the DQ pins at the first rising edge of the DQS following the preamble. The tDQSS specification must be satisfied for write cycles. The subsequent burst bit data are issued on successive edges of the DQS until the burst length is completed, which is 4 or 8 bit burst. When the burst has finished, any additional data supplied to the DQ pins will be ignored. The DQ Signal is ignored after the burst write operation is complete. The time from the completion of the burst write to bank precharge is the write recovery time (WR).
DDR2 SDRAM pin timings are specified for either single ended mode or differential mode depending on the setting of the EMRS "Enable DQS" mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timings are measured is mode dependent. In single ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at VREF. In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, $\overline{DQS}$. This distinction in timing methods is guaranteed by design and characterization. Note that when differential data strobe mode is disabled via the EMRS, the complementary pin, $\overline{DQS}$, must be tied externally to VSS through a 20 ohm to 10 Kohm resistor to insure proper operation.

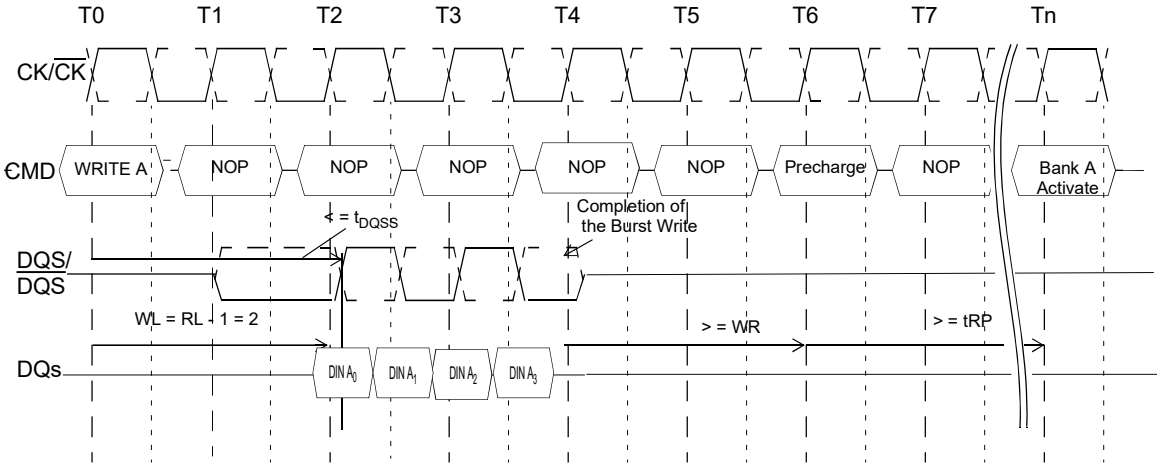


Data input (write) timing

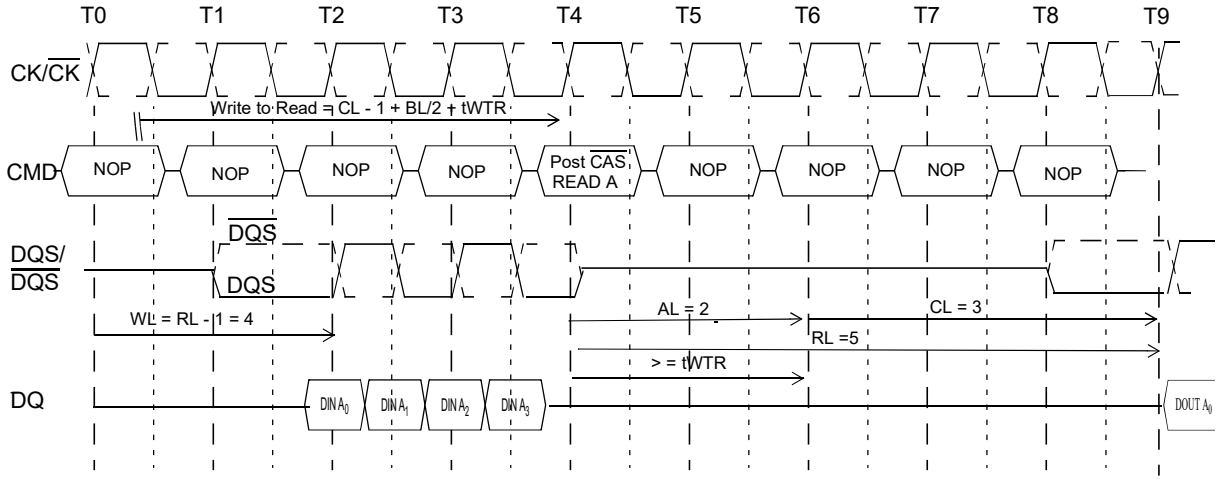
Burst Write Operation: RL = 5, WL = 4, tWR = 3 (AL=2, CL=3), BL = 4



Burst Write Operation: RL = 3, WL = 2, tWR = 2 (AL=0, CL=3), BL = 4

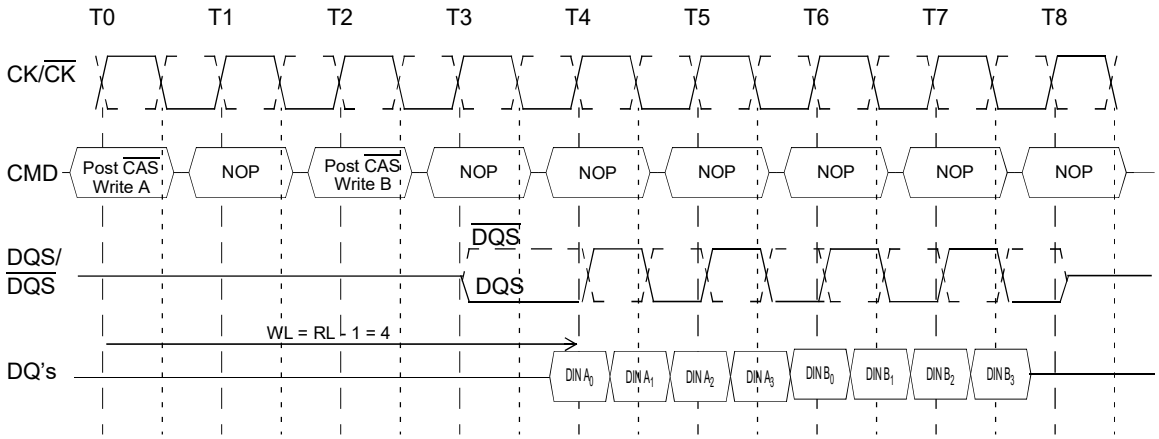


Burst Write followed by Burst Read: RL = 5 (AL=2, CL=3), WL = 4, tWTR = 2, BL = 4



The minimum number of clock from the burst write command to the burst read command is [CL - 1 + BL/2 + tWTR]. This tWTR is not a write recovery time (tWR) but the time required to transfer the 4bit write data from the input buffer into sense amplifiers in the array. tWTR is defined in AC spec table of this data sheet.

Seamless Burst Write Operation: RL = 5, WL = 4, BL = 4

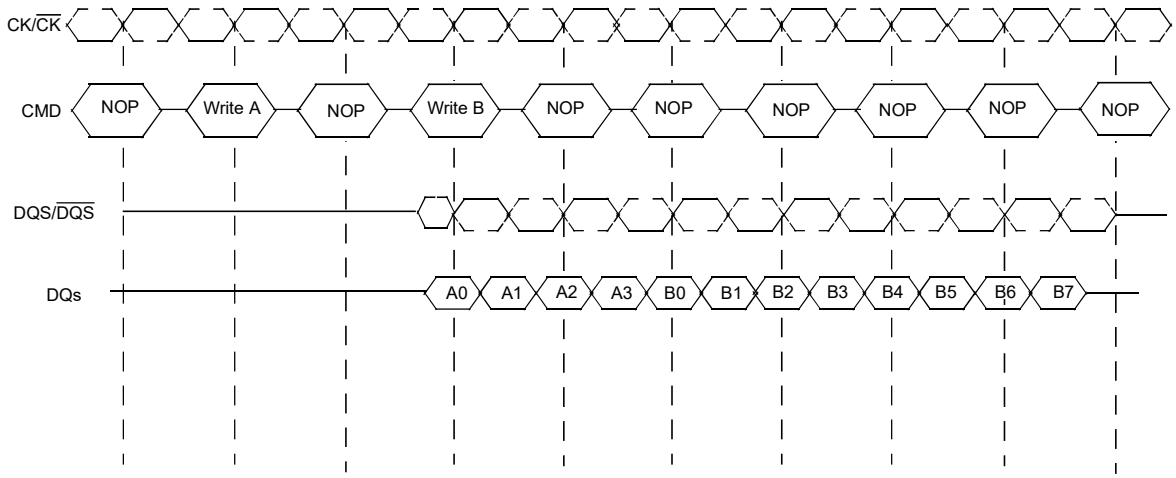


The seamless burst write operation is supported by enabling a write command every other clock for BL = 4 operation, every four clocks for BL = 8 operation. This operation is allowed regardless of same or different banks as long as the banks are activated

Writes interrupted by a write

Burst write can only be interrupted by another write with 4 bit burst boundary. Any other case of write interrupt is not allowed.

Write Burst Interrupt Timing Example: (CL=3, AL=0, RL=3, WL=2, BL=8)

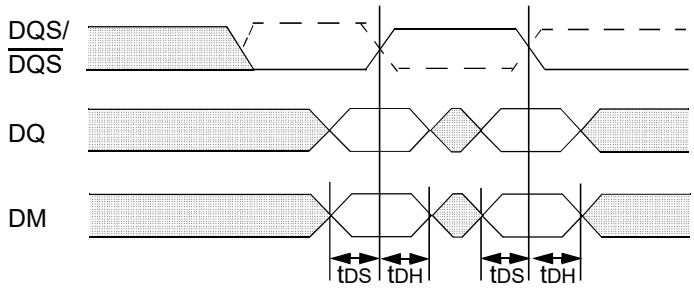


Notes:
1. Write burst interrupt function is only allowed on burst of 8. Burst interrupt of 4 is prohibited.
2. Write burst of 8 can only be interrupted by another Write command. Write burst interruption by Read command or Precharge command is prohibited.
3. Write burst interrupt must occur exactly two clocks after previous Write command. Any other Write burst interrupt timings are prohibited.
4. Write burst interruption is allowed to any bank inside DRAM.
5. Write burst with Auto Precharge enabled is not allowed to interrupt.
6. Write burst interruption is allowed by another Write with Auto Precharge command.
7. All command timings are referenced to burst length set in the mode register. They are not referenced to actual burst. For example, minimum Write to Precharge timing is WL+BL/2+tWR where tWR starts with the rising clock after the un-interrupted burst end and not from the end of actual burst end.

2.4.5 Write Data Mask

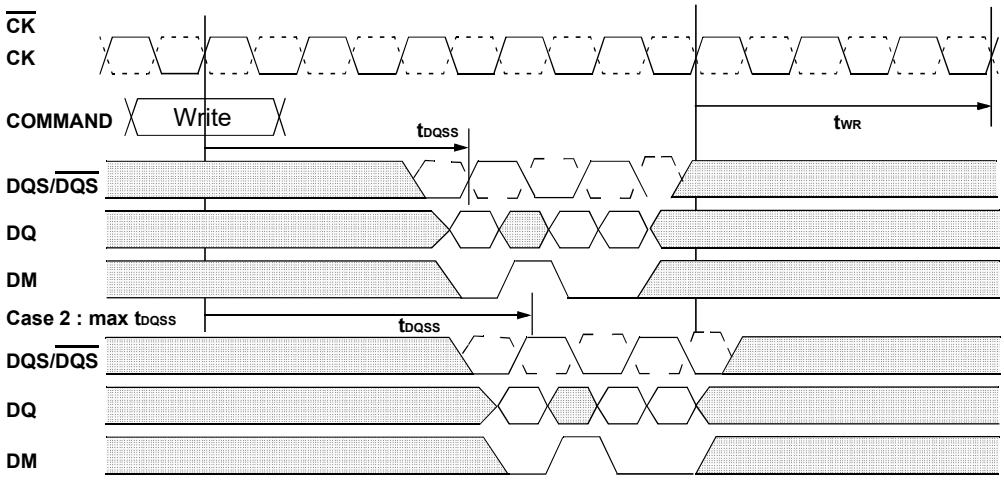
One write data mask (DM) pin for each 8 data bits (DQ) will be supported on DDR2 SDRAMs, Consistent with the implementation on DDR SDRAMs. It has identical timings on write operations as the data bits, and though used in a uni-directional manner, is internally loaded identically to data bits to insure matched system timing. DM of x4 and x16 bit organization is not used during read cycles.

Data Mask Timing



Data Mask Function, WL=3, AL=0, BL = 4 shown

Case 1 : min t_{DQSS}



2.5 Precharge Operation

The Precharge Command is used to precharge or close a bank that has been activated. The Precharge Command is triggered when $\overline{CS}$, $\overline{RAS}$ and $\overline{WE}$ are LOW and $\overline{CAS}$ is HIGH at the rising edge of the clock. The Precharge Command can be used to precharge each bank independently or all banks simultaneously. Three address bits A10, BA0 and BA1 for 512Mb and four address bits A10, BA0~BA2 for 1Gb and higher densities are used to define which bank to precharge when the command is issued. For 8 bank devices, refer to Bank Active section of this data sheet.

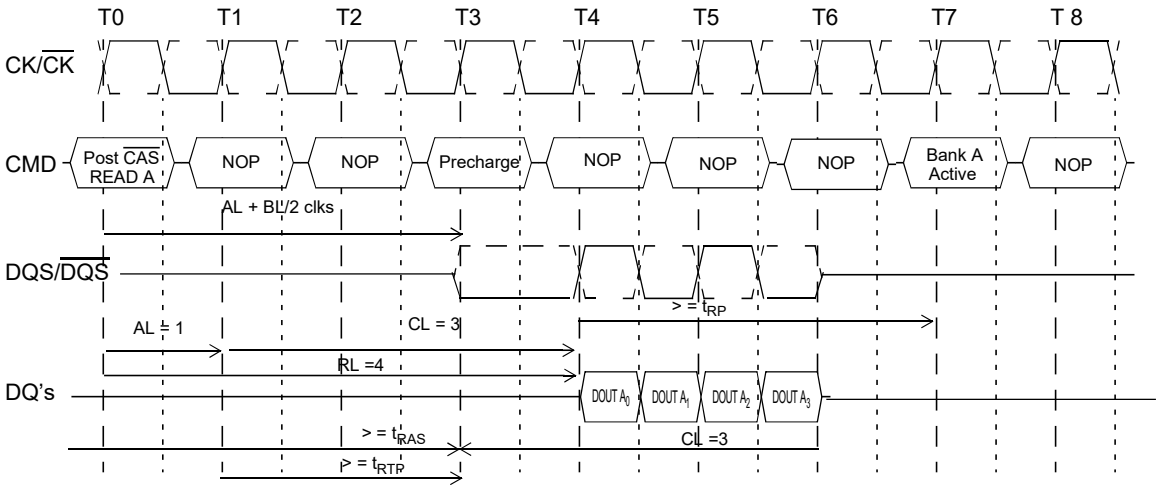
Bank Selection for Precharge by Address Bits

A10	BA2	BA1	BA0	Precharged Bank(s)	Remarks
LOW	LOW	LOW	LOW	Bank 0 only	
LOW	LOW	LOW	HIGH	Bank 1 only	
LOW	LOW	HIGH	LOW	Bank 2 only	
LOW	LOW	HIGH	HIGH	Bank 3 only	
LOW	HIGH	LOW	LOW	Bank 4 only	1Gb and higher
LOW	HIGH	LOW	HIGH	Bank 5 only	1Gb and higher
LOW	HIGH	HIGH	LOW	Bank 6 only	1Gb and higher
LOW	HIGH	HIGH	HIGH	Bank 7only	1Gb and higher
HIGH	DON'T CARE	DON'T CARE	DON'T CARE	All Banks	

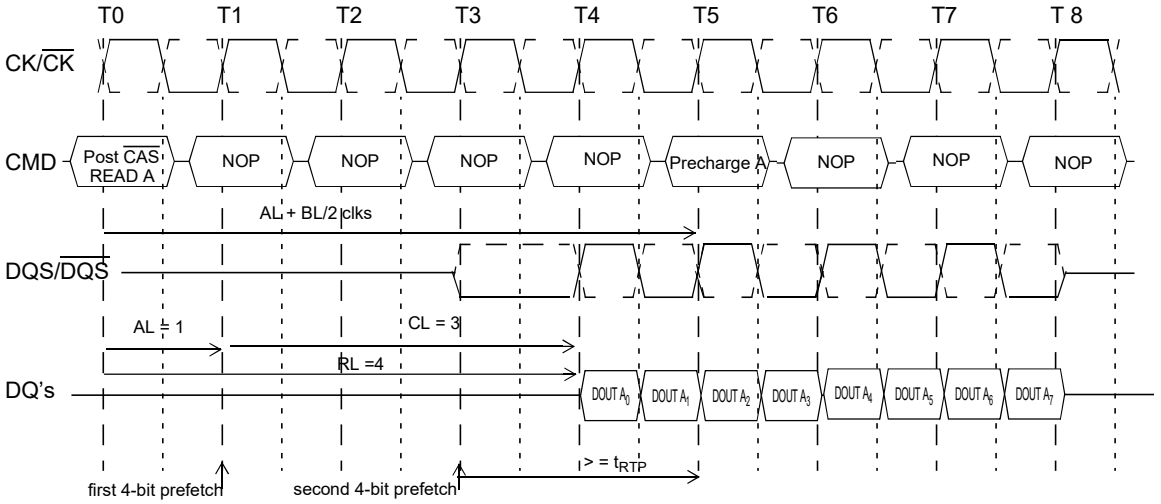
Burst Read Operation Followed by Precharge

Minium Read to precharge command spacing to the same bank = AL + BL/2 clocks
For the earliest possible precharge, the precharge command may be issued on the rising edge which is "Additive latency(AL) + BL/2 clocks" after a Read command. A new bank active (command) may be issued to the same bank after the RAS precharge time (t_{RP}). A precharge command cannot be issued until t_{RAS} is satisfied.
The minimum Read to Precharge spacing has also to satisfy a minimum analog time from the rising clock egde that initiates the last 4-bit prefetch of a Read to Precharge command. This time is called tRTP (Read to Precharge). For BL = 4 this is the time from the actual read (AL after the Read command) to Precharge command. For BL = 8 this is the time from AL + 2 clocks after the Read to the Precharge command.

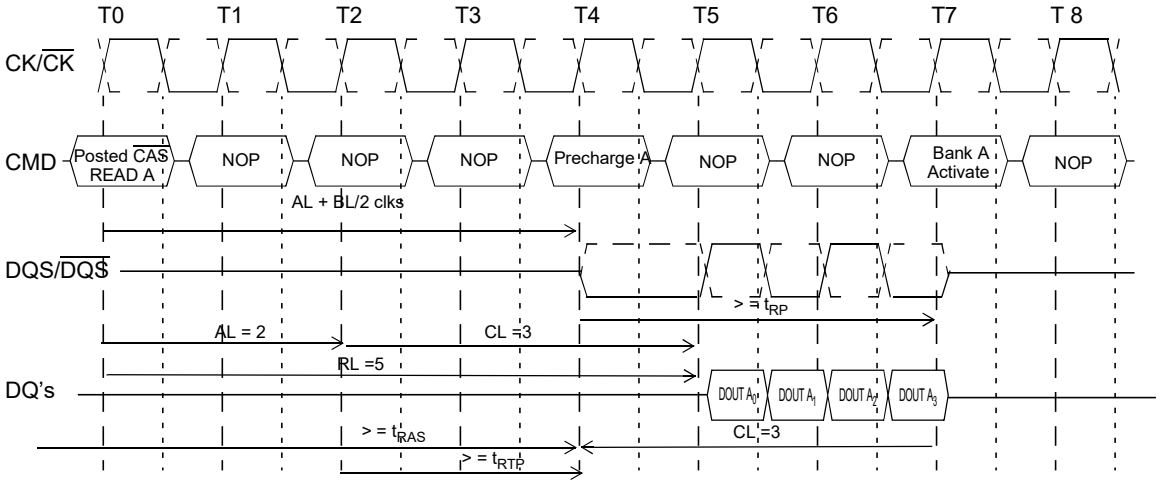
Example 1: Burst Read Operation Followed by Precharge: RL = 4, AL = 1, CL = 3, BL = 4, t_{RTP} <= 2 clocks



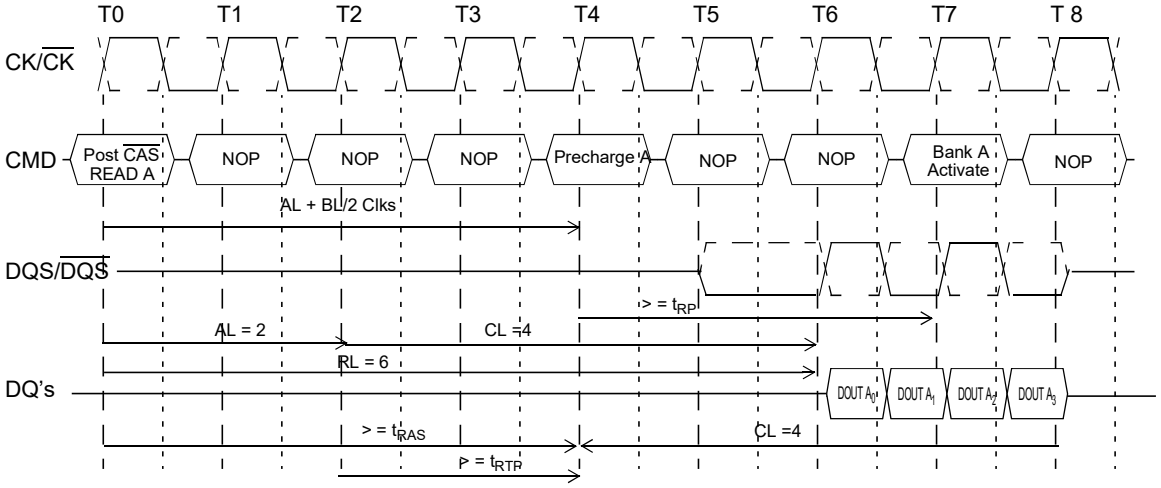
Example 2: Burst Read Operation Followed by Precharge: RL = 4, AL = 1, CL = 3, BL = 8, t_{RTP} <= 2 clocks



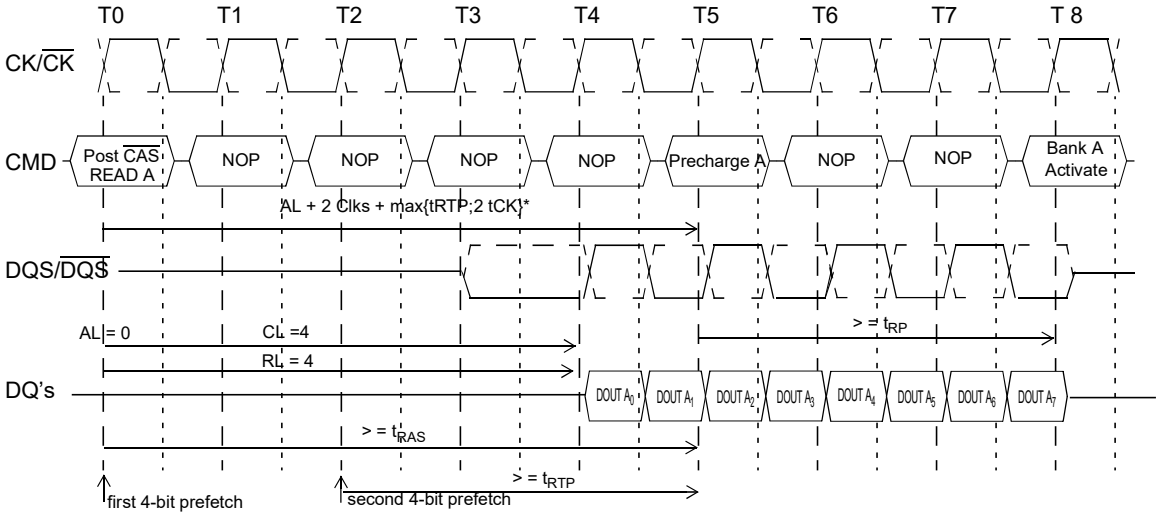
Example 3: Burst Read Operation Followed by Precharge: RL = 5, AL = 2, CL = 3, BL = 4, t_{RTP} <= 2 clocks



Example 4: Burst Read Operation Followed by Precharge: RL = 6, AL = 2, CL = 4, BL = 4, t_{RTP} <= 2 clocks



Example 5: Burst Read Operation Followed by Precharge: RL = 4, AL = 0, CL = 4, BL = 8, t_{RTP} > 2 clocks

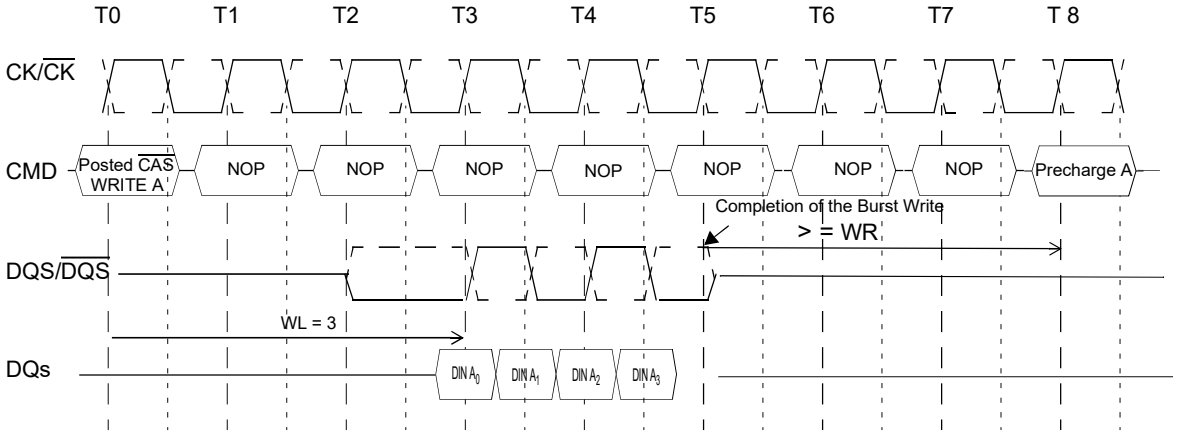


* : rounded to next interger

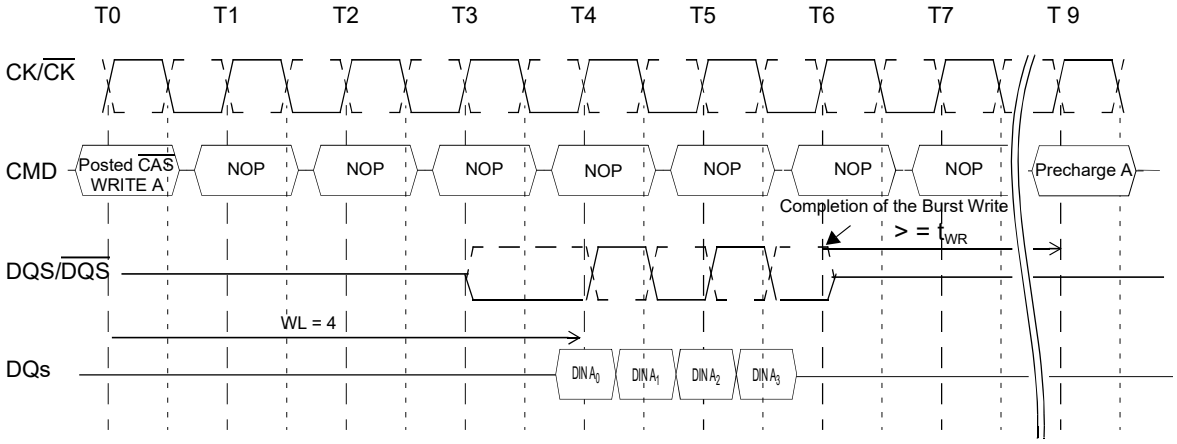
Burst Write followed by Precharge

Minium Write to Precharge Command spacing to the same bank = WL + BL/2 clks + tWR
For write cycles, a delay must be satisfied from the completion of the last burst write cycle until the Precharge Command can be issued. This delay is known as a write recovery time (tWR) referenced from the completion of the burst write to the precharge command. No Precharge command should be issued prior to the tWR delay.

Example 1: Burst Write followed by Precharge: WL = (RL-1) =3



Example 2: Burst Write followed by Precharge: WL = (RL-1) = 4



2.6 Auto Precharge Operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the Precharge command or the auto-precharge function. When a Read or a Write command is given to the DDR2 SDRAM, the CAS timing accepts one extra address, column address A10, to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle. If A10 is low when the READ or WRITE command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst sequence. If A10 is high when the Read or Write command is issued, then the auto-precharge function is engaged. During auto-precharge, a Read command will execute as normal with the exception that the active bank will begin to precharge on the rising edge which is CAS latency (CL) clock cycles before the end of the read burst.

Auto-precharge is also implemented during Write commands. The precharge operation engaged by the Auto precharge command will not begin until the last data of the burst write sequence is properly stored in the memory array.

This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon CAS latency) thus improving system performance for random data access. The RAS lockout circuit internally delays the Precharge operation until the array restore operation has been completed (tRAS satisfied) so that the auto precharge command may be issued with any read or write command.

Burst Read with Auto Precharge

If A10 is high when a Read Command is issued, the Read with Auto-Precharge function is engaged. The DDR2 SDRAM starts an Auto Precharge operation on the rising edge which is (AL + BL/2) cycles later than the read with AP command if tRAS(min) and tRTP are satisfied.

If tRAS(min) is not satisfied at the edge, the start point of auto-precharge operation will be delayed until tRAS(min) is satisfied.

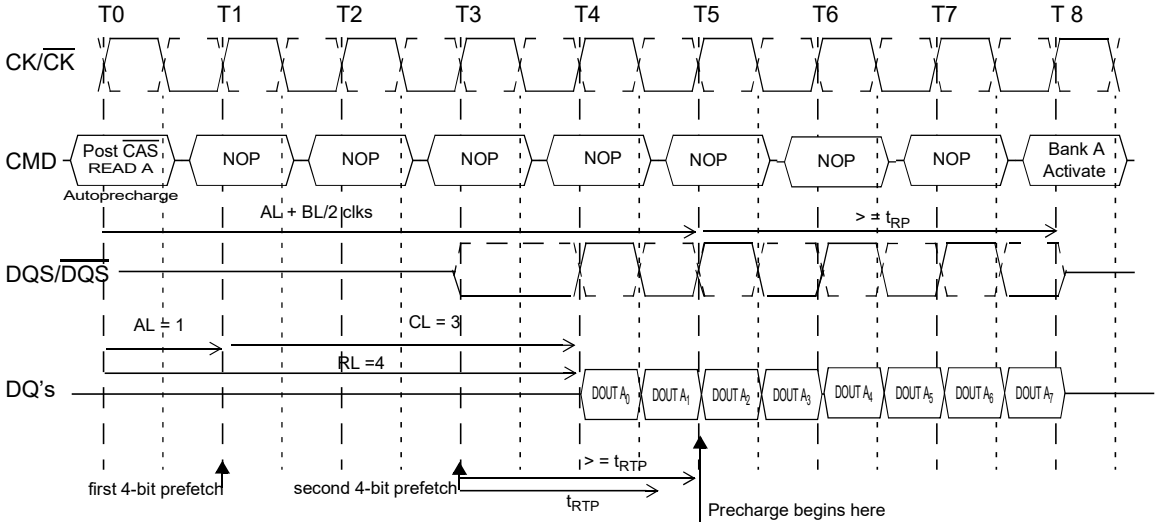
If tRTP(min) is not satisfied at the edge, the start point of auto-precharge operation will be delayed until tRTP(min) is satisfied.
In case the internal precharge is pushed out by tRTP, tRP starts at the point where the internal precharge happens (not at the next rising clock edge after this event). So for BL = 4 the minimum time from Read_AP to the next Activate command becomes AL + (tRTP + tRP)* (see example 2) for BL = 8 the time from Read_AP to the next Activate is AL + 2 + (tRTP + tRP)*, where “*” means: “rounded up to the next integer”.
In any event internal precharge does not start earlier than two clocks after the last 4-bit prefetch.

A new bank activate (command) may be issued to the same bank if the following two conditions are satisfied simultaneously.

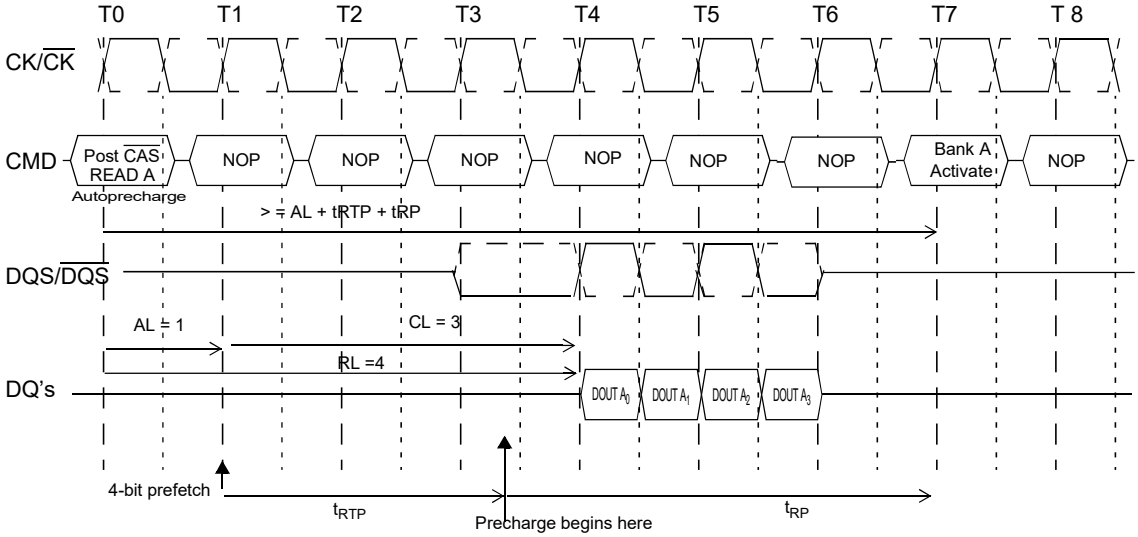
(1) The RAS precharge time (tRP) has been satisfied from the clock at which the auto precharge begins.

(2) The RAS cycle time (tRC) from the previous bank activation has been satisfied.

Example 1: Burst Read Operation with Auto Precharge:
RL = 4, AL = 1, CL = 3, BL = 8, t_{RTP} <= 2 clocks

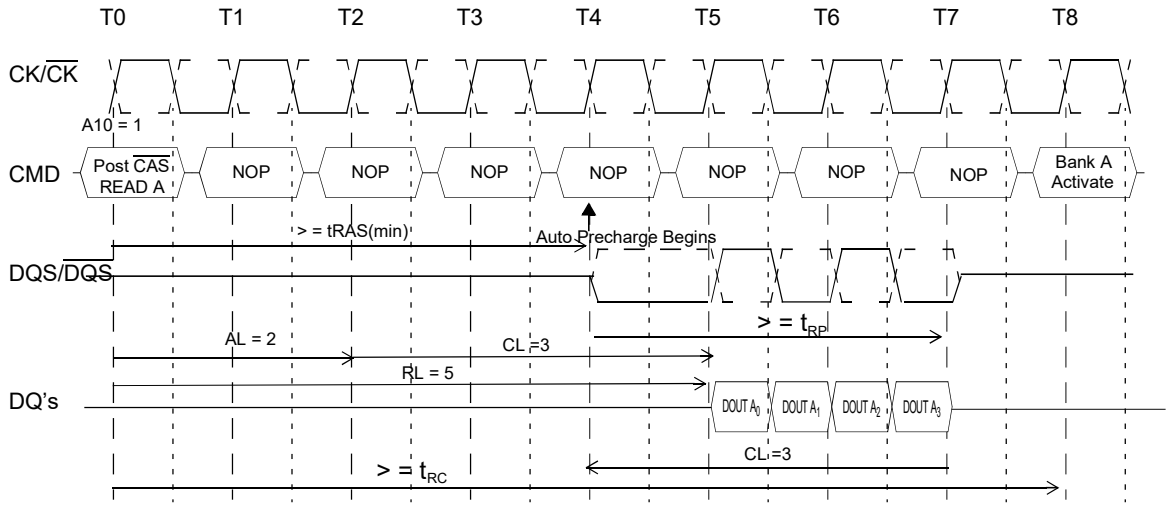


Example 2: Burst Read Operation with Auto Precharge:
RL = 4, AL = 1, CL = 3, BL = 4, t_{RTP} > 2 clocks



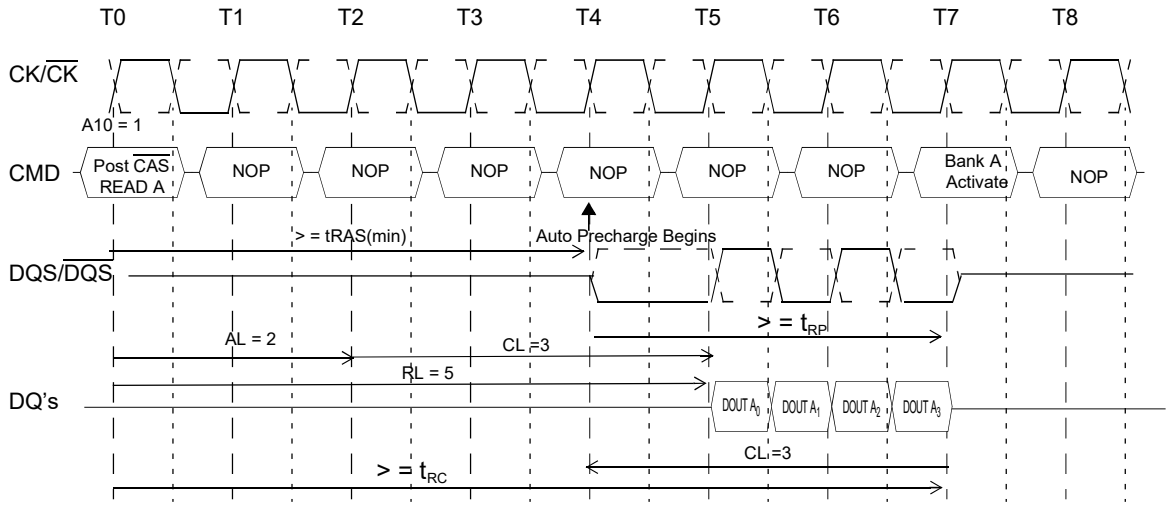
Example 3: Burst Read with Auto Precharge Followed by an activation to the Same Bank(tRC Limit):

RL = 5 (AL = 2, CL = 3, internal tRCD = 3, BL = 4, t_{RTP} <= 2 clocks)



Example 4: Burst Read with Auto Precharge Followed by an Activation to the Same Bank(tRP Limit):

RL = 5 (AL = 2, CL = 3, internal tRCD = 3, BL = 4, t_{RTP} <= 2 clocks)



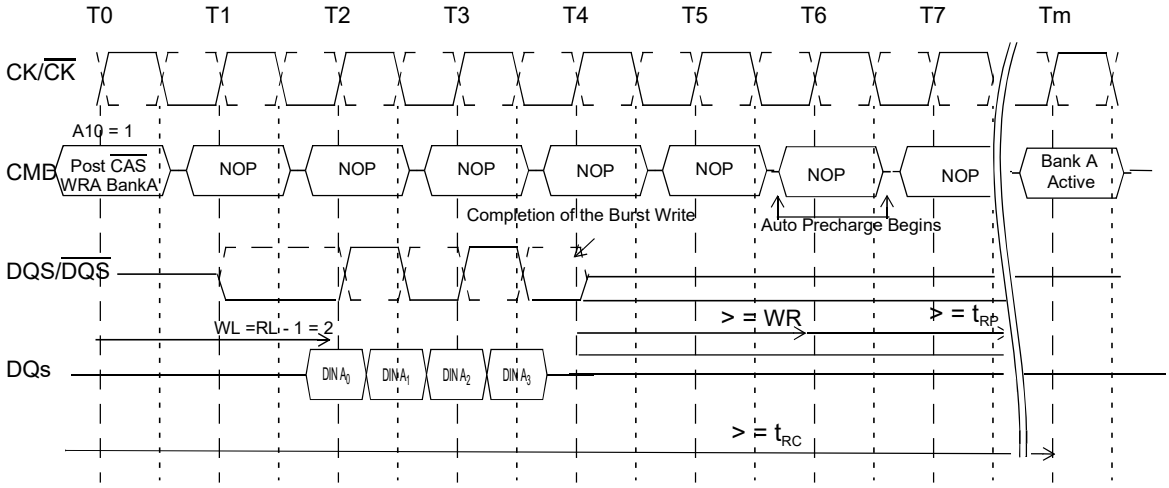
Burst Write with Auto-Precharge

If A10 is high when a Write Command is issued, the Write with Auto-Precharge function is engaged. The DDR2 SDRAM automatically begins precharge operation after the completion of the burst write plus write recovery time (tWR). The bank undergoing auto-precharge from the completion of the write burst may be reactivated if the following two conditions are satisfied.

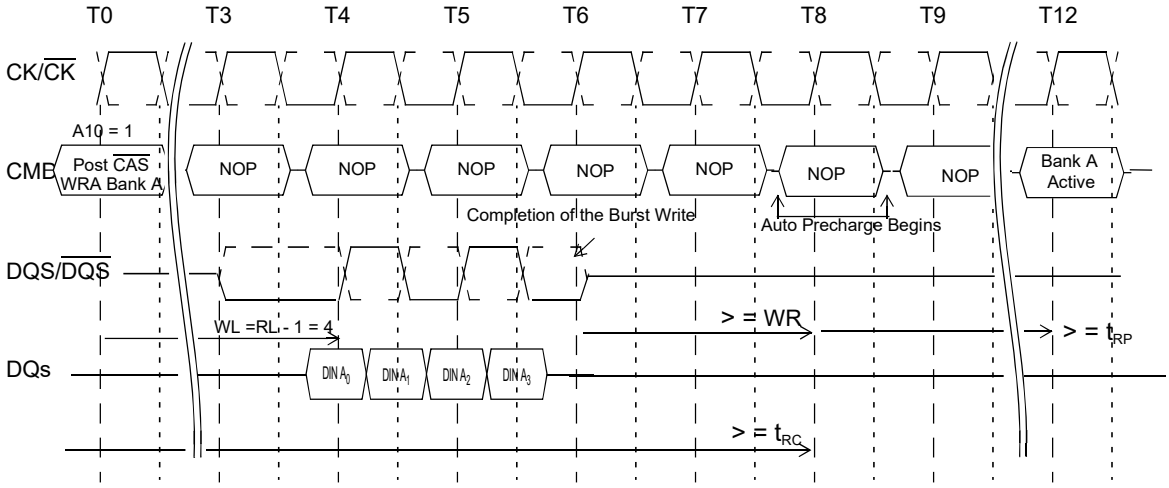
(1) The data-in to bank activate delay time (WR + tRP) has been satisfied.

(2) The $\overline{RAS}$ cycle time (tRC) from the previous bank activation has been satisfied.

Burst Write with Auto-Precharge (tRC Limit): WL = 2, tWR =2, BL = 4, tRP=3



Burst Write with Auto-Precharge (tWR + tRP): WL = 4, tWR =2, BL = 4, tRP=3



2.7 Refresh Commands

DDR2 SDRAMs require a refresh of all rows in any rolling 64 ms interval. Each refresh is generated in one of two ways: by an explicit Auto-Refresh command, or by an internally timed event in SELF REFRESH mode. Dividing the number of device rows into the rolling 64ms interval, tREFI, which is a guideline to controllers for distributed refresh timing. For example, a 512Mb DDR2 SDRAM has 8192 rows resulting in a tREFI of 7.8μs. To avoid excessive interruptions to the memory controller, higher density DDR2 SDRAMS maintain 7.8μs average refresh time and perform multiple internal refresh bursts. In these cases, the refresh recovery times, tRFC an tXSNR are extended to accomodate these internal operations.

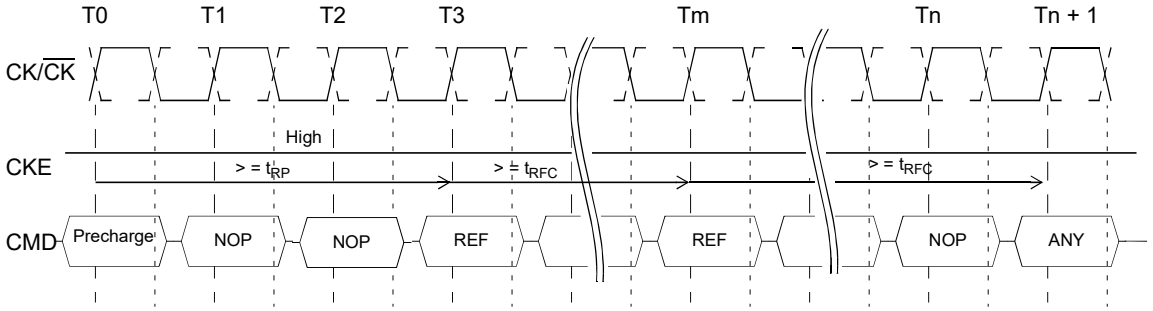
2.7.1 Auto Refresh Command

AUTO REFRESH is used during normal operation of the DDR2 SDRAM. This command is nonpersistent, so it must be issued each time a refresh is required. The refresh addressing is generated by the internal refresh controller. This makes the address bits “Don’t Care” during an AUTO REFRESH command.

When CS, RAS and CAS are held low and $\overline{WE}$ high at the rising edge of the clock, the chip enters the Refresh mode (REF). All banks of the DDR2 SDRAM must be precharged and idle for a minimum of the Precharge time (tRP) before the Refresh command (REF) can be applied. An address counter, internal to the device, supplies the bank address during the refresh cycle. No control of the external address bus is required once this cycle has started.

When the refresh cycle has completed, all banks of the DDR2 SDRAM will be in the precharged (idle) state. A delay between the Refresh command (REF) and the next Activate command or subsequent Refresh command must be greater than or equal to the Refresh cycle time (tRFC).

To allow for improved efficiency in scheduling andswitching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight Refresh commands can be posted to any given DDR2 SDRAM, meaning that the maximum absolute interval between any Refresh command and the next Refresh command is 9 * tREFI.



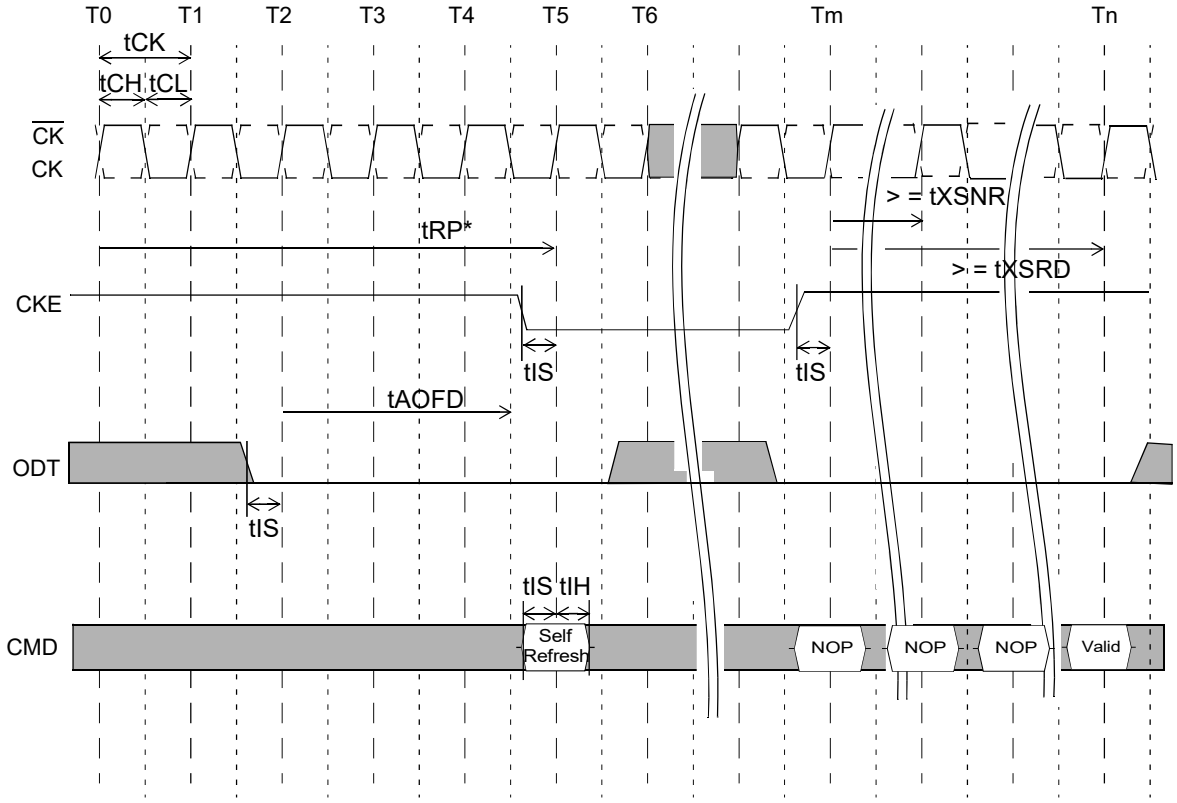
2.7.2 Self Refresh Operation

The Self Refresh command can be used to retain data in the DDR2 SDRAM, even if the rest of the system is powered down. When in the Self Refresh mod, the DDR2 SDRAM retains data without external clocking.

The DDR2 SDRAM device has a built-in timer to accommodate Self Refresh operation. The Self Refresh Command is defined by having CS, RAS, CAS and CKE held low with WE high at the rising edge of the clock. ODT must be turned off before issuing Self Refresh command, by either driving ODT pin low or using EMRS command. Once the Command is registered, CKE must be held low to keep the device in Self Refresh mode. The DLL is automatically disabled upon entering Self Refresh and is automatically enabled upon existing Self Refresh. When the DDR2 SDRAM has entered Self Refresh mode all of the external signals except CKE, are “don’t care”. The DRAM initiates a minimum of one Auto Refresh command internally within tCKE period once it enters Self Refresh mode.The clock is internally disabled during Self Refresh Operation to save power. The minimum time that the DDR2 SDRAM must remain in Self Refresh mode is tCKE. The user may change the external clock frequency or halt the external clock one clock after Self-Refresh entry is registered, however, the clock must be restarted and stable before the device can exit Self Refresh operation.

The procedure for existing Self Refresh requires a sequence of commands. First, the clock must be stable prior to CKE going back HIGH. Once Self Refresh Exit command is registered, a delay equal or longer than the tXSNR or tXSRD must be satisfied before a valid command can be issued to the device. CKE must remain high for the entire Self Refresh exit period tXSRD for proper operation. Upon exit from Self Refresh, the DDR2 SDRAM can be put back into Self Refresh mode after tXSRD expires.NOP or deselect commands must be registered on each positive clock edge during the Self Refresh exit interval. ODT should also be turned off during tXSRD.

The Use of Self Refresh mode introduce the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self Refresh mode. Upon exit from Self Refresh, the DDR2 SDRAM requires a minimum of one extra auto refresh command before it is put back into Self Refresh mode.



- Device must be in the “All banks idle” state prior to entering Self Refresh mode.
- ODT must be turned off tAOFD before entering Self Refresh mode, and can be turned on again when tXSRD timing is satisfied.
- tXSRD is applied for a Read or a Read with autoprecharge command
- tXSNR is applied for any command except a Read or a Read with autoprecharge command.

2.8 Power-Down

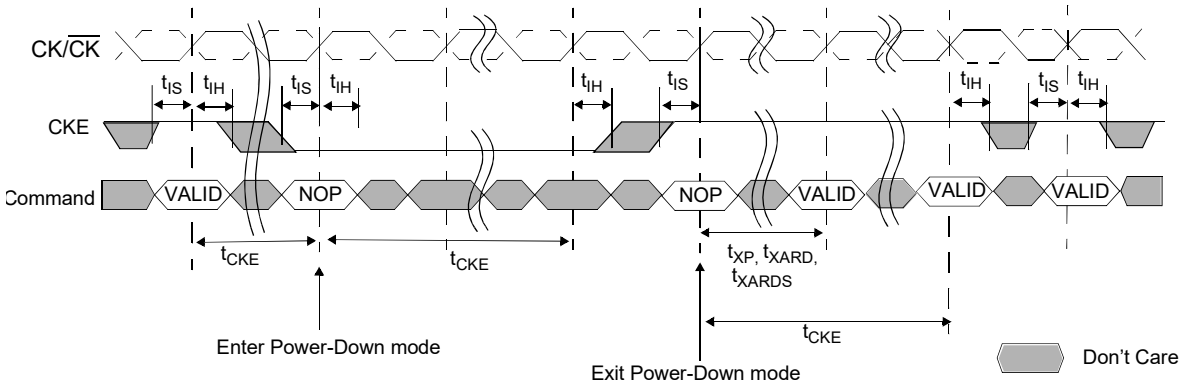
Power-down is synchronously entered when CKE is registered low (along with Nop or Deselect command). CKE is not allowed to go low while mode register or extended mode register command time, or read or write operation is in progress. CKE is allowed to go low while any of other operations such as row activation, precharge or auto-precharge, or auto-refresh is in progress, but power-down IDD spec will not be applied until finishing those operations. Timing diagrams are shown in the following pages with details for entry into power down.

The DLL should be in a locked state when power-down is entered. Otherwise DLL should be reset after exiting power-down mode for proper read operation.

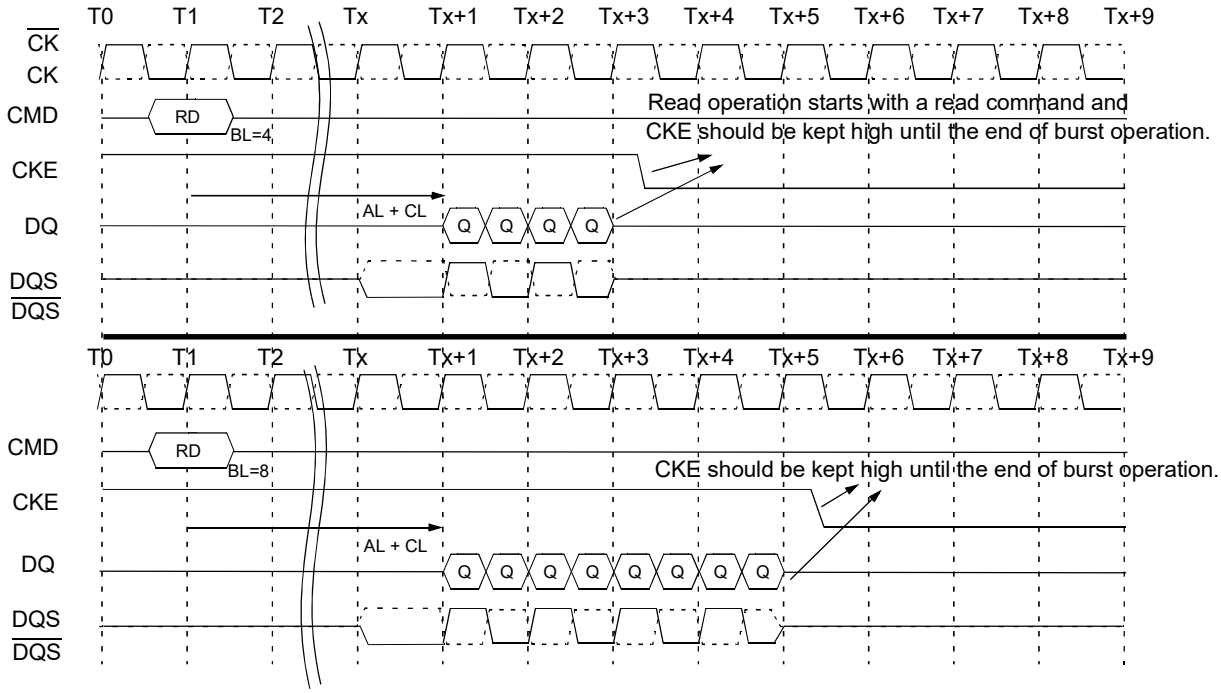
If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CK, $\overline{CK}$, ODT and CKE. Also the DLL is disabled upon entering precharge power-down or slow exit active power-down, but the DLL is kept enabled during fast exit active power-down. In power-down mode, CKE low and a stable clock signal must be maintained at the inputs of the DDR2 SDRAM, and ODT should be in a valid state but all other input signals are “Don’t Care”. CKE low must be maintained until tCKE has been satisfied. Power-down duration is limited by 9 times tREFI of the device.

The power-down state is synchronously exited when CKE is registered high (along with a Nop or Deselect command). CKE high must be maintained until tCKE has been satisfied. A valid, executable command can be applied with power-down exit latency, tXP, tXARD, or tXARDS, after CKE goes high. Power-down exit latency is defined at AC spec table of this data sheet.

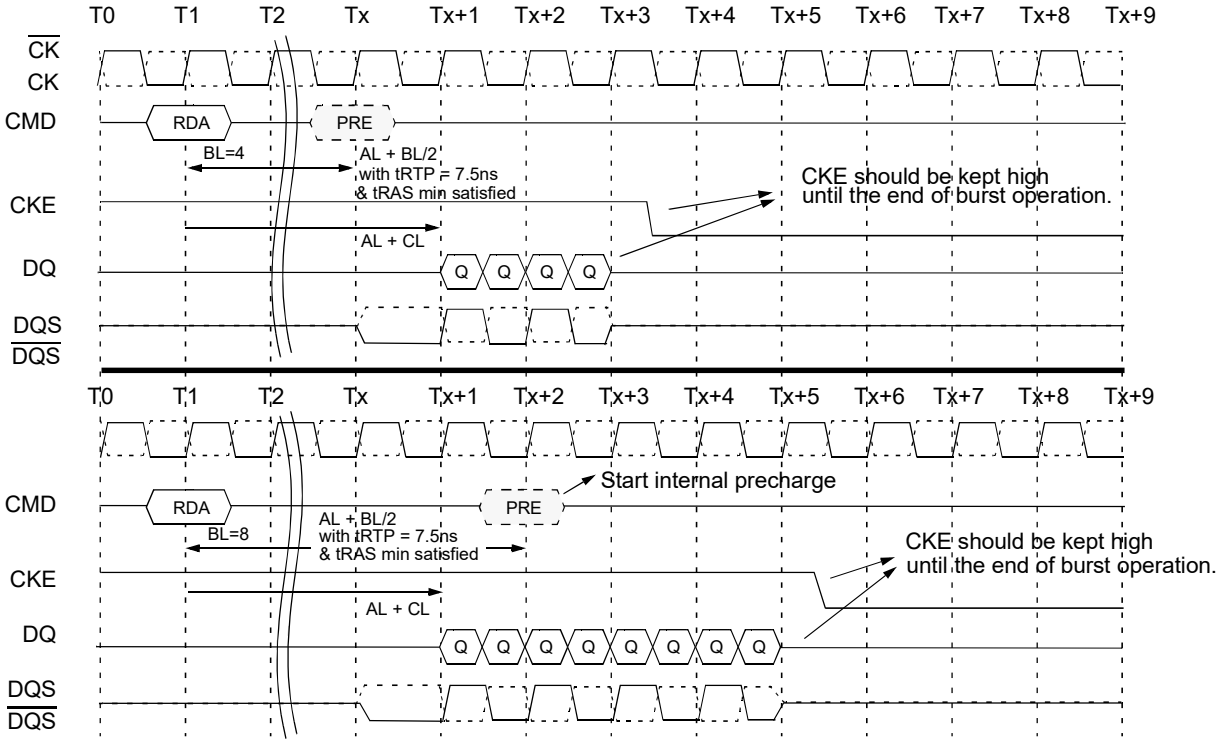
Basic Power Down Entry and Exit timing diagram



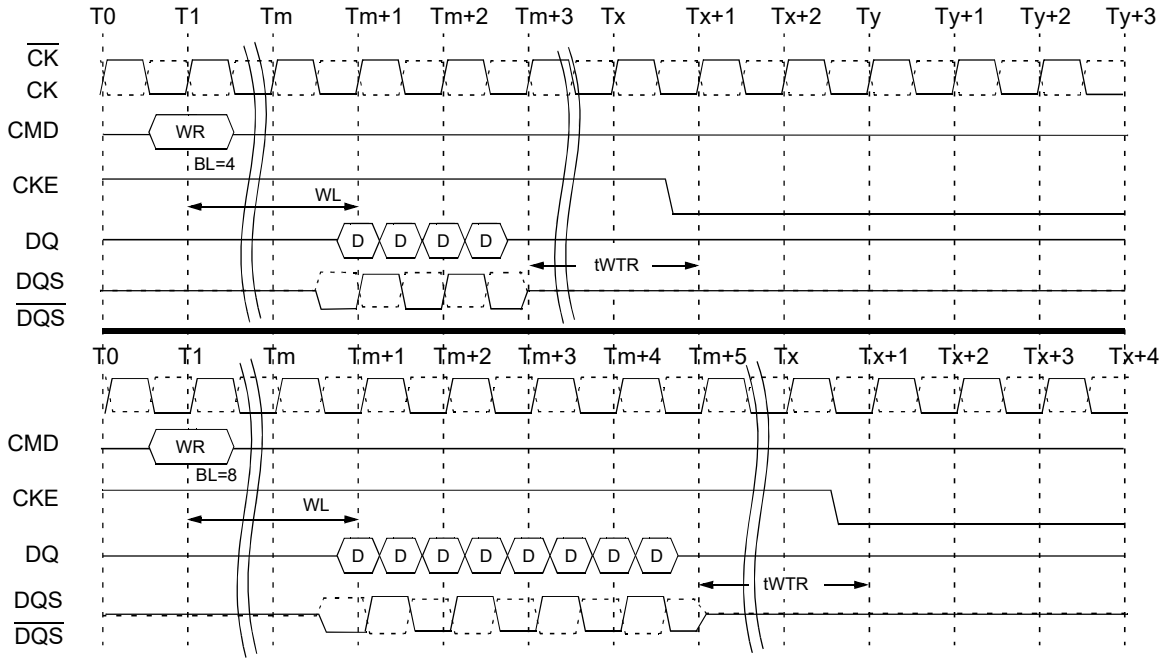
Read to power down entry



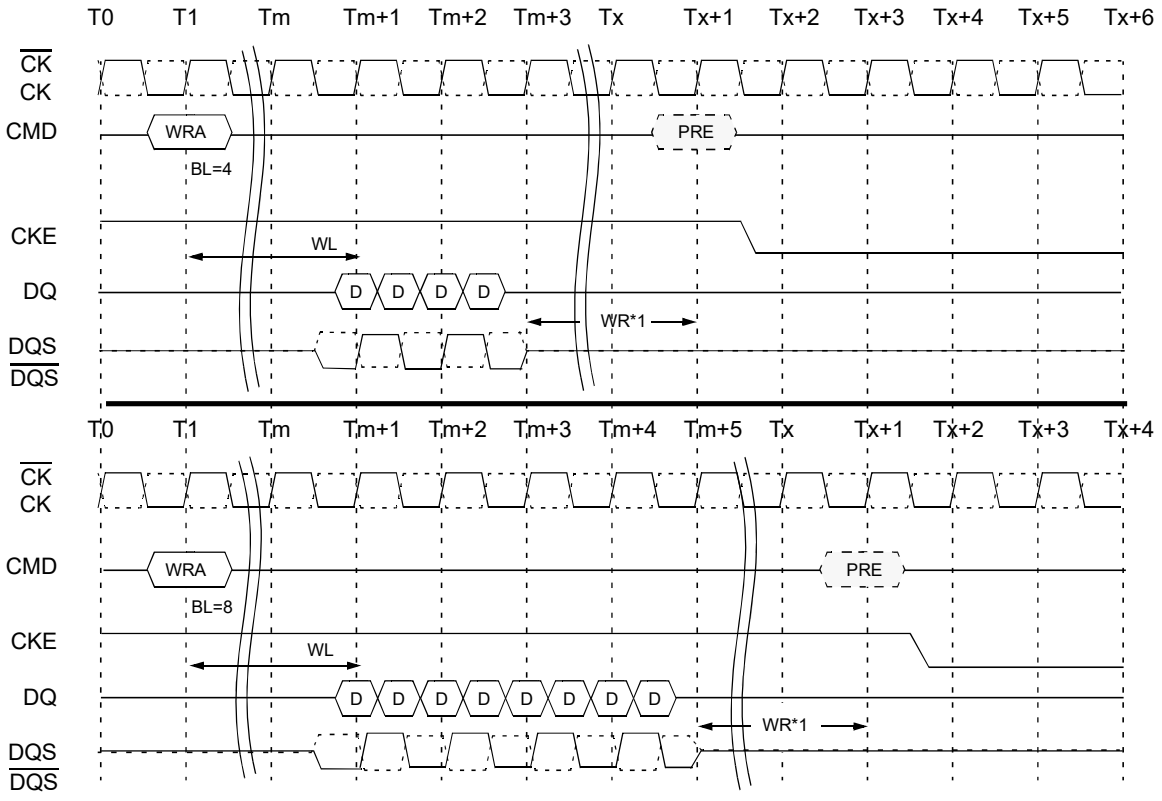
Read with Autoprecharge to power down entry



Write to power down entry

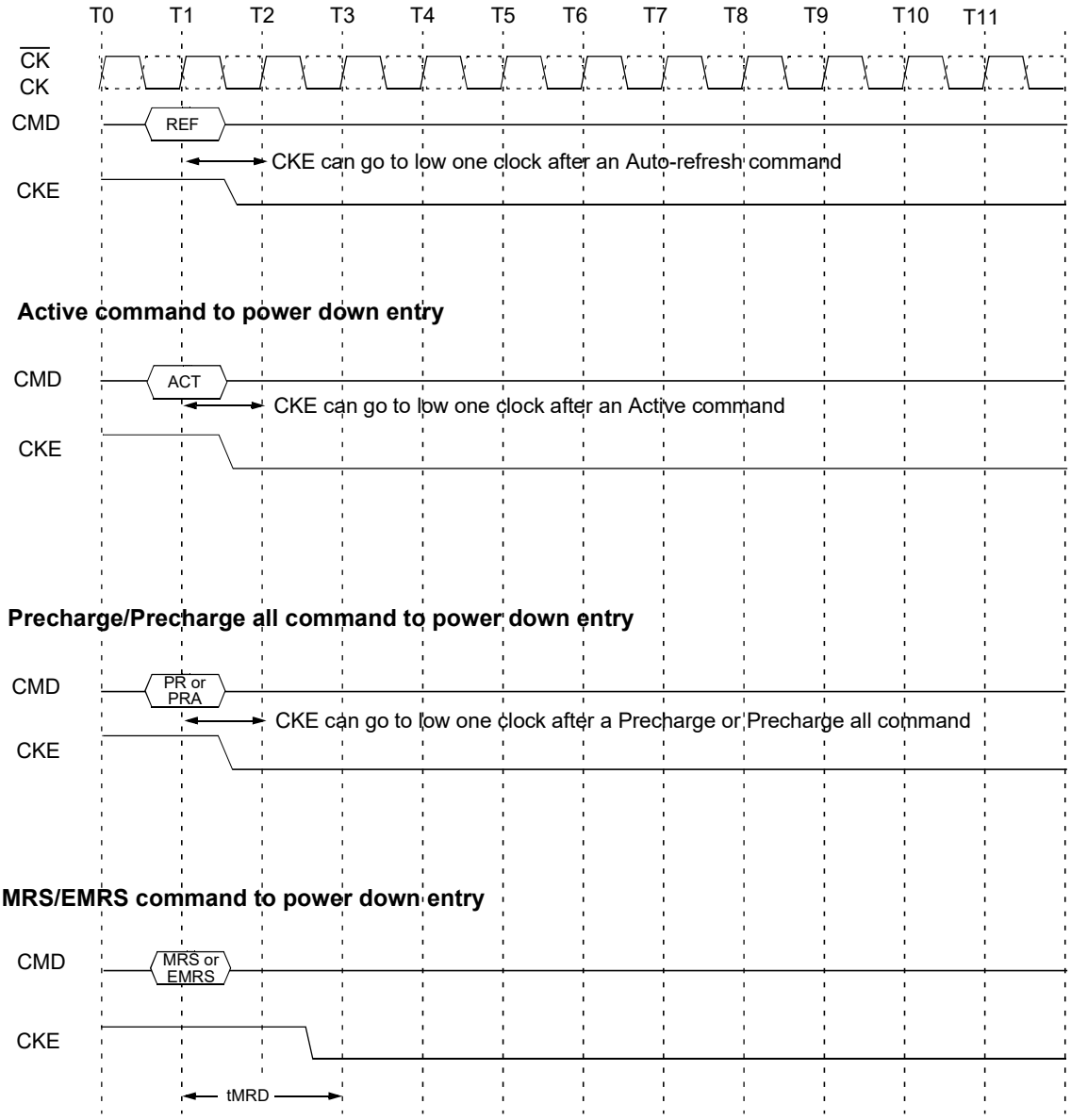


Write with Autoprecharge to power down entry



* 1: WR is programmed through MRS

Refresh command to power down entry



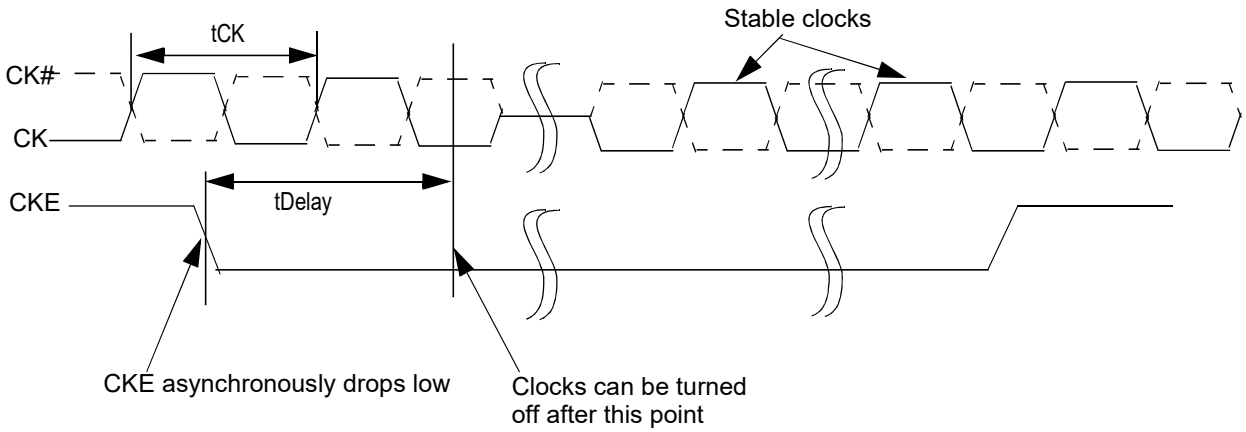
Active command to power down entry

Precharge/Precharge all command to power down entry

MRS/EMRS command to power down entry

2. 9 Asynchronous CKE Low Event

DRAM requires CKE to be maintained “HIGH” for all valid operations as defined in this data sheet. If CKE asynchronously drops “LOW” during any valid operation DRAM is not guaranteed to preserve the contents of array. If this event occurs, memory controller must satisfy DRAM timing specification tDelay before turning off the clocks. Stable clocks must exist at the input of DRAM before CKE is raised “HIGH” again. DRAM must be fully re-initialized (steps 4 thru 13) as described in initializaliation sequence. DRAM is ready for normal operation after the initialization sequence. See AC timing parametric table for tDelay specification

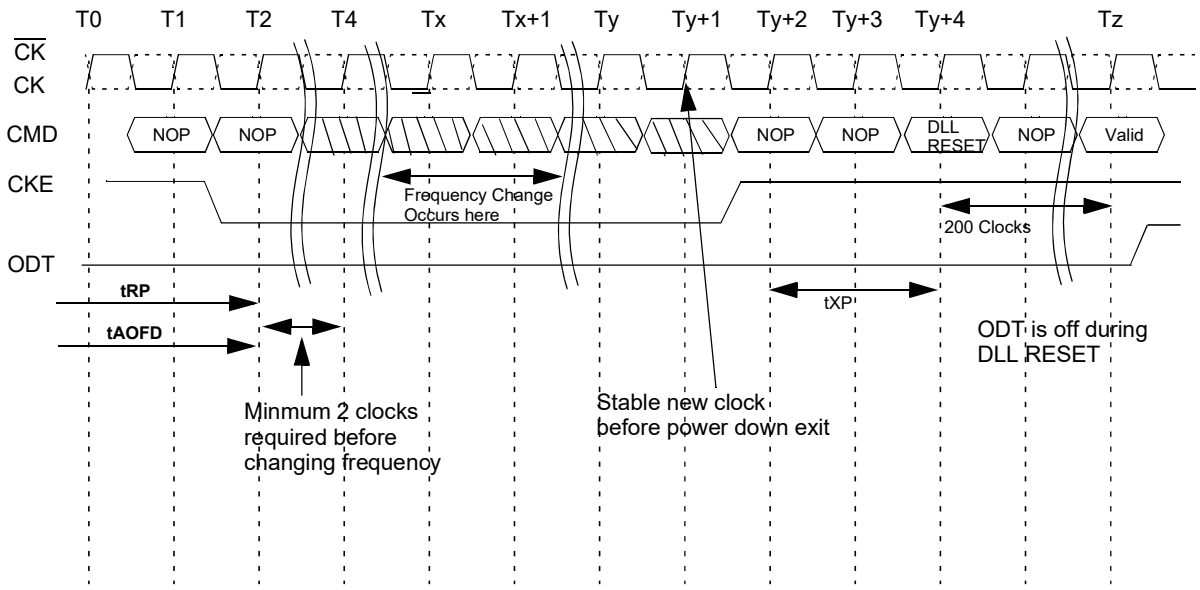


Input Clock Frequency Change during Precharge Power Down

DDR2 SDRAM input clock frequency can be changed under following condition:

DDR2 SDRAM is in precharged power down mode. ODT must be turned off and CKE must be at logic LOW level. A minimum of 2 clocks must be waited after CKE goes LOW before clock frequency may change. SDRAM input clock frequency is allowed to change only within minimum and maximum operating frequency specified for the particular speed grade. During input clock frequency change, ODT and CKE must be held at stable LOW levels. Once input clock frequency is changed, stable new clocks must be provided to DRAM before precharge power down may be exited and DLL must be RESET via EMRS after precharge power down exit. Depending on new clock frequency an additional MRS command may need to be issued to appropriately set the WR, CL etc.. During DLL re-lock period, ODT must remain off. After the DLL lock time, the DRAM is ready to operate with new clock frequency.

Clock Frequency Change in Precharge Power Down Mode



2.10 No Operation Command

The No Operation command should be used in cases when the DDR2 SDRAM is in an idle or a wait state. The purpose of the No Operation command (NOP) is to prevent the DDR2 SDRAM from registering any unwanted commands between operations. A No Operation command is registered when $\overline{CS}$ is low with $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ held high at the rising edge of the clock. A No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

2.11 Deselect Command

The Deselect command performs the same function as a No Operation command. Deselect command occurs when $\overline{CS}$ is brought high at the rising edge of the clock, the $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ signals become don't cares.

3. Truth Tables

3.1 Command truth table.

Function	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0 BA1 BA2	A15-A11	A10	A9 - A0	Notes
	Previous Cycle	Current Cycle									
(Extended) Mode Register	H	H	L	L	L	L	BA	OP Code			1,2
Refresh (REF)	H	H	L	L	L	H	X	X	X	X	1
Self Refresh Entry	H	L	L	L	L	H	X	X	X	X	1
Self Refresh Exit	L	H	H	X	X	X	X	X	X	X	1,7
			L	H	H	H					
Single Bank Precharge	H	H	L	L	H	L	BA	X	L	X	1,2
Precharge all Banks	H	H	L	L	H	L	X	X	H	X	1
Bank Activate	H	H	L	L	H	H	BA	Row Address			1,2
Write	H	H	L	H	L	L	BA	Column	L	Column	1,2,3,
Write with Auto Precharge	H	H	L	H	L	L	BA	Column	H	Column	1,2,3,
Read	H	H	L	H	L	H	BA	Column	L	Column	1,2,3
Read with Auto-Precharge	H	H	L	H	L	H	BA	Column	H	Column	1,2,3
No Operation	H	X	L	H	H	H	X	X	X	X	1
Device Deselect	H	X	H	X	X	X	X	X	X	X	1
Power Down Entry	H	L	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					
Power Down Exit	L	H	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					

1. All DDR2 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock.
2. Bank addesses BA0, BA1, BA2 (BA) determine which bank is to be operated upon. For (E)MR BA selects an (Extended) Mode Register.
3. Burst reads or writes at BL=4 cannot be terminated or interrupted. See sections "Reads interrupted by a Read" and "Writes interrupted by a Write" in section 1.4 for details.
4. The Power Down Mode does not perform any refresh operations. The duration of Power Down is therefore limited by the refresh requirements outlined in section 1.2.2.
5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh. See section 1.2.2.4.
6. “X” means “H or L (but a defined logic level)”.
7. Self refresh exit is asynchronous.
8. VREF must be maintained during Self Refresh operation

Table 6. Command truth table

3.2 Clock Enable (CKE) Truth Table for Synchronous Transitions

Current State [2]	CKE		Command (N) [3]	Action (N) [3]	Notes
	Previous Cycle [1] (N-1)	Current Cycle [1] (N)	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$		
Power Down	L	L	X	Maintain Power-Down	11, 13, 15
	L	H	DESELECT or NOP	Power Down Exit	4, 8, 11,13
Self Refresh	L	L	X	Maintain Self Refresh	11, 15
	L	H	DESELECT or NOP	Self Refresh Exit	4, 5,9
Bank(s) Active	H	L	DESELECT or NOP	Active Power Down Entry	4,8,10,11,13
All Banks Idle	H	L	DESELECT or NOP	Precharge Power Down Entry	4, 8, 10,11,13
	H	L	REFRESH	Self Refresh Entry	6, 9, 11,13
	H	H	Refer to the Command Truth Table		7

Notes:

1. CKE (N) is the logic state of CKE at clock edge N; CKE (N–1) was the state of CKE at the previous clock edge.
2. Current state is the state of the DDR SDRAM immediately prior to clock edge N.
3. COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N).
4. All states and sequences not shown are illegal or reserved unless explicitely described elsewhere in this document.
5. On Self Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the t_{XSNR} period. Read commands may be issued only after t_{XSRD} (200 clocks) is satisfied.
6. Self Refresh mode can only be entered from the All Banks Idle state.
7. Must be a legal command as defined in the Command Truth Table.
8. Valid commands for Power Down Entry and Exit are NOP and DESELECT only.
9. Valid commands for Self Refresh Exit are NOP and DESELECT only.
10. Power Down and Self Refresh can not be entered while Read or Write operations, (Extended) Mode Register Set operations or Precharge operations are in progress. See section 2.2.9 "Power Down" and 2.2.8 "Self Refresh Command" for a detailed list of restrictions.
11. Minimum CKE high time is three clocks.; minimum CKE low time is three clocks.
12. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh. See section 2.2.2.4.
13. The Power Down does not perform any refresh operations. The duration of Power Down Mode is therefore limited by the refresh requirements outlined in section 2.2.7.
14. CKE must be maintained high while the SDRAM is in OCD calibration mode .
15. “X” means “don’t care (including floating around VREF)” in Self Refresh and Power Down. However ODT must be driven high or low in Power Down if the ODT fucntion is enabled (Bit A2 or A6 set to “1” in EMRS(1)).

3.3 Data Mask Truth Table

Name (Functional)	DM	DQs	Note
Write enable	L	Valid	1
Write inhibit	H	X	1
1. Used to mask write data, provided coinsident with the corresponding data			

4. Operation Conditions

4.1 Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	- 1.0 V ~ 2.3 V	V	1
VDDQ	Voltage on VDDQ pin relative to Vss	- 0.5 V ~ 2.3 V	V	1
VDDL	Voltage on VDDL pin relative to Vss	- 0.5 V ~ 2.3 V	V	1
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	- 0.5 V ~ 2.3 V	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1, 2
II	Input leakage current; any input 0V VIN VDD; all other balls not under test = 0V)	-2 uA ~ 2 uA	uA	
IOZ	Output leakage current; 0V VOUT VDDQ; DQ and ODT disabled	-5 uA ~ 5 uA	uA	

Note:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions. please refer to JESD51-2 standard.

4.2 Operating Temperature Condition

Symbol	Parameter	Rating	Units	Notes
T_{OPER}	Operating Temperature	0 to 95	°C	1

1. Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
2. At 0 - 85°C, operation temperature range are the temperature which all DRAM specification will be supported.
3. At 85~95°C operation temperature range, doubling refresh commands in frequency to a 32ms period (tREFI=3.9us) is required, and to enter to self refresh mode at this temperature range, and EMRS command is required to change internal refresh rate.

4.3 Thermal Characteristics

PARAMETER	Description	Value (Ta=25℃)	Value (Ta=70℃)	UNIT	NOTES
TC	Case Temperature	41	86	℃	7
TJ	Junction Temperature	43	88	℃	7
Theta_JA	Thermal resistance junction to ambient	69.6	69.6	℃/W	1,2,3,4,5,7
Theta_JC	Thermal resistance junction to case	6.07	6.07	℃/W	1,2,6,7

1. Measurement procedures for each parameter must follow standard procedures defined in the current JEDEC JESD-51 standared.
2. Theta_JA and Theta_JC must be measured with the high effective thermal conductivity test board defined in JESD51-7
3. Airflow information must be deocumented for Theta_JA.
4. Theta_JA should only be used for comparing the thermal performance of signle packages and not for system related junction.
5. Theta_JA is the natural convection junction-to-ambient air thermal resistance measured in one cubic foot sealed enclosure as described in JESD-51. The environment is sometimes referred to as "still-air" although natural convection causes the air to move.
6. Theta_JC case surface is defined as the "outside surface of the package (case) closest to the chip mounting area when that same surface is properly hear sunk" so as to minimize temperature variation across that surface.
7. Test condition : Voltage 1.8V / Frequency : 400Mhz

5. AC & DC Operating Conditions

5.1 DC Operating Conditions

5.1.1 Recommended DC Operating Conditions (SSTL_1.8)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.7	1.8	1.9	V	1
VDDL	Supply Voltage for DLL	1.7	1.8	1.9	V	1,2
VDDQ	Supply Voltage for Output	1.7	1.8	1.9	V	1,2
VREF	Input Reference Voltage	0.49*VDDQ	0.50*VDDQ	0.51*VDDQ	mV	3,4
VTT	Termination Voltage	VREF-0.04	VREF	VREF+0.04	V	5

Note:

1. Min. Typ. and Max. values increase by 100mV for 400Mhz speed option.
2. VDDQ tracks with VDD,VDDL tracks with VDD. AC parameters are measured with VDD,VDDQ and VDD.
3. The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ
4. Peak to peak ac noise on VREF may not exceed +/-2% VREF (dc).
5. VTT of transmitting device must track VREF of receiving device.

5.1.2 ODT DC electrical characteristics

PARAMETER/CONDITION	SYMBOL	MIN	NOM	MAX	UNITS	NOTES
Rtt effective impedance value for EMR(A6,A2)=0,1; 75 ohm	Rtt1(eff)	60	75	90	ohm	1
Rtt effective impedance value for EMR(A6,A2)=1,0; 150 ohm	Rtt2(eff)	120	150	180	ohm	1
Rtt effective impedance value for EMR(A6,A2)=1,1; 50 ohm	Rtt3(eff)	40	50	60	ohm	1
Deviation of VM with respect to VDDQ/2	delta VM	-6		+6	%	1

Note :

1. Test condition for Rtt measurements

Measurement Definition for Rtt(eff): Apply V_{IH} (ac) and V_{IL} (ac) to test pin separately, then measure current $I(V_{IH}(ac))$ and $I(V_{IL}(ac))$ respectively. V_{IH} (ac), V_{IL} (ac), and VDDQ values defined in SSTL_18

$$Rtt(eff) = \frac{V_{IH}(ac) - V_{IL}(ac)}{I(V_{IH}(ac)) - I(V_{IL}(ac))}$$

Measurement Definition for VM : Measurement Voltage at test pin(mid point) with no load.

$$\text{delta VM} = \left(\frac{2 \times Vm}{VDDQ} - 1\right) \times 100\%$$

5.2 DC & AC Logic Input Levels

5.2.1 Input DC Logic Level

Symbol	Parameter	Min.	Max.	Units	Notes
V_{IH}(dc)	dc input logic HIGH	VREF + 0.125	VDDQ + 0.3	V	
V_{IL}(dc)	dc input logic LOW	- 0.3	VREF - 0.125	V	

5.2.2 Input AC Logic Level

Symbol	Parameter	Min.	Max.	Units	Notes
V_{IH} (ac)	ac input logic HIGH	VREF + 0.250	-	V	1
V_{IL} (ac)	ac input logic LOW	-	VREF - 0.250	V	1

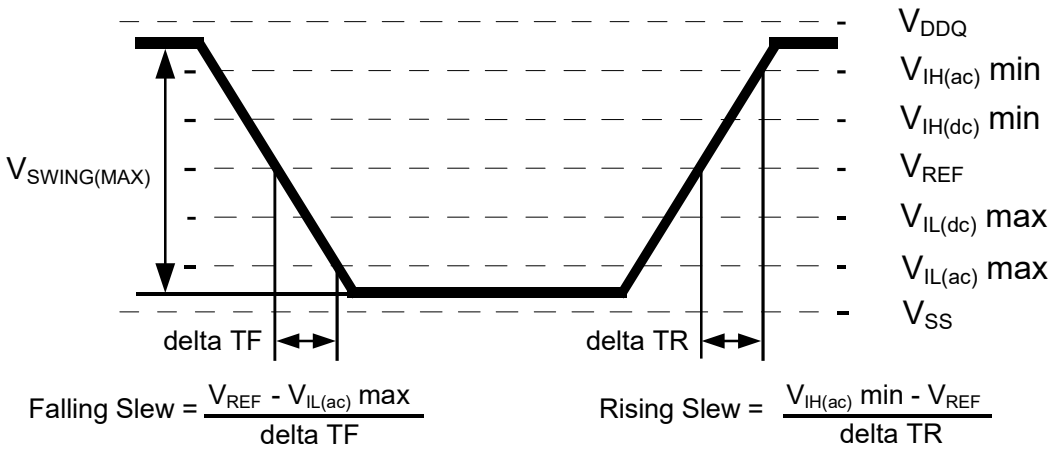
Note : 1. 400Mhz at 1.8V supported

5.2.3 AC Input Test Conditions

Symbol	Condition	Value	Units	Notes
V_{REF}	Input reference voltage	0.5 * V_{DDQ}	V	1
$V_{SWING(MAX)}$	Input signal maximum peak to peak swing	1.0	V	1
SLEW	Input signal minimum slew rate	1.0	V/ns	2, 3

Note:

1. Input waveform timing is referenced to the input signal crossing through the V_{REF} level applied to the device under test.
2. The input signal minimum slew rate is to be maintained over the range from V_{REF} to $V_{IH(ac)}$ min for rising edges and the range from V_{REF} to $V_{IL(ac)}$ max for falling edges as shown in the figure below.
3. AC timings are referenced with input waveforms switching from VIL(ac) to VIH(ac) on the positive transitions and VIH(ac) to VIL(ac) on the negative transitions.



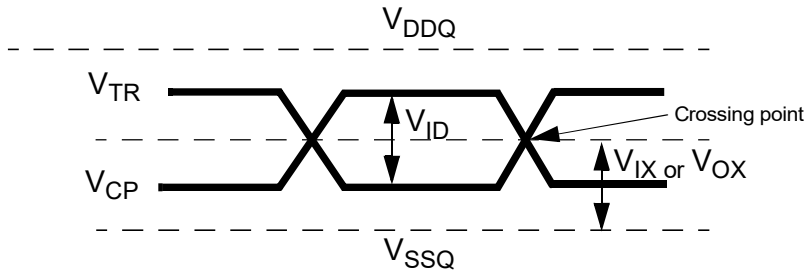
< Figure : AC Input Test Signal Waveform>

5.2.4 Differential Input AC logic Level

Symbol	Parameter	Min.	Max.	Units	Notes
V_{ID} (ac)	ac differential input voltage	0.5	VDDQ + 0.6	V	1
V_{IX} (ac)	ac differential cross point voltage	0.5 * VDDQ - 0.175	0.5 * VDDQ + 0.175	V	2

Note:

1. VIN(DC) specifies the allowable DC execution of each input of differential pair such as CK, $\overline{CK}$, DQS, $\overline{DQS}$, LDQS, $\overline{LDQS}$, UDQS and $\overline{UDQS}$.
2. VID(DC) specifies the input differential voltage |VTR -VCP | required for switching, where VTR is the true input (such as CK, DQS, LDQS or UDQS) level and VCP is the complementary input (such as $\overline{CK}$, $\overline{DQS}$, $\overline{LDQS}$ or $\overline{UDQS}$) level.
   The minimum value is equal to VIH(DC) - V IL(DC).



< Differential signal levels >

Note:

1. VID(AC) specifies the input differential voltage |VTR -VCP | required for switching, where VTR is the true input signal
   (such as CK, DQS, LDQS or UDQS) and VCP is the complementary input signal (such as $\overline{CK}$, $\overline{DQS}$, $\overline{LDQS}$ or $\overline{UDQS}$).
   The minimum value is equal to V IH(AC) - V IL(AC).
2. The typical value of VIX(AC) is expected to be about 0.5 * VDDQ of the transmitting device and VIX(AC) is expected to track variations in VDDQ. VIX(AC) indicates the voltage at which differential input signals must cross.

5.2.5 Differential AC output parameters

Symbol	Parameter	Min.	Max.	Units	Notes
V_{OX} (ac)	ac differential cross point voltage	0.5 * VDDQ - 0.125	0.5 * VDDQ + 0.125	V	1

Note:

1. The typical value of VOX(AC) is expected to be about 0.5 * V DDQ of the transmitting device and VOX(AC) is expected to track variations in VDDQ. VOX(AC) indicates the voltage at which differential output signals must cross.

5.3 Output Buffer Characteristics

5.3.1 Output AC Test Conditions

Symbol	Parameter	SSTL_18 Class II	Units	Notes
V_{OH}	Minimum Required Output Pull-up under AC Test Load	V_{TT} + 0.603	V	
V_{OL}	Maximum Required Output Pull-down under AC Test Load	V_{TT} - 0.603	V	
V_{OTR}	Output Timing Measurement Reference Level	0.5 * V_{DDQ}	V	1

Note:

1. The VDDQ of the device under test is referenced.

5.3.2 Output DC Current Drive

Symbol	Parameter	SSTI_18	Units	Notes
$I_{OH(dc)}$	Output Minimum Source DC Current	- 13.4	mA	1, 3, 4
$I_{OL(dc)}$	Output Minimum Sink DC Current	13.4	mA	2, 3, 4

Note:

1. V_{DDQ} = 1.7 V; V_{OUT} = 1420 mV. (V_{OUT} - V_{DDQ})/I_{OH} must be less than 21 ohm for values of V_{OUT} between V_{DDQ} and V_{DDQ} - 280 mV.
2. V_{DDQ} = 1.7 V; V_{OUT} = 280 mV. V_{OUT}/I_{OL} must be less than 21 ohm for values of V_{OUT} between 0 V and 280 mV.
3. The dc value of V_{REF} applied to the receiving device is set to V_{TT}
4. The values of $I_{OH(dc)}$ and $I_{OL(dc)}$ are based on the conditions given in Notes 1 and 2. They are used to test device drive current capability to ensure V_{IH} min plus a noise margin and V_{IL} max minus a noise margin are delivered to an SSTL_18 receiver. The actual current values are derived by shifting the desired driver operating point (see Section 3.3) along a 21 ohm load line to define a convenient driver current for measurement.

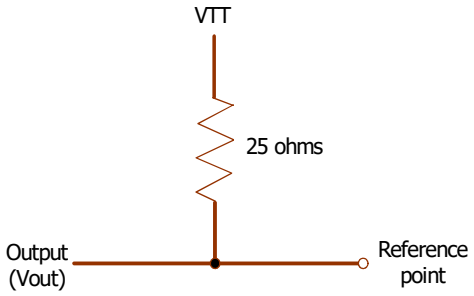
5.3.3 OCD default characteristics

Description	Parameter	Min	Nom	Max	Unit	Notes
Output impedance		-	-	-	ohms	1
Output impedance step size for OCD calibration		0		1.5	ohms	6
Pull-up and pull-down mismatch		0		4	ohms	1,2,3
Output slew rate	Sout	1.5	-	5	V/ns	1,4,5,6,7,8

Note :

1. Absolute Specifications (Toper; VDD = +1.8V ±0.1V, VDDQ = +1.8V ±0.1V)
2. Impedance measurement condition for output source dc current: VDDQ=1.7V; VOUT=1420mV; (VOUT-VDDQ)/Ioh must be less than 23.4 ohms for values of VOUT between VDDQ and VDDQ-280mV.
   Impedance measurement condition for output sink dc current: VDDQ = 1.7V; VOUT = 280mV; VOUT/Iol must be less than 23.4 ohms for values of VOUT between 0V and 280mV.
3. Mismatch is absolute value between pull-up and pull-dn, both are measured at same temperature and voltage.
4. Slew rate measured from vil(ac) to vih(ac).
5. The absolute value of the slew rate as measured from DC to DC is equal to or greater than the slew rate as measured from AC to AC. This is guaranteed by design and characterization.
6. This represents the step size when the OCD is near 18 ohms at nominal conditions across all process corners/variations and represents only the DRAM uncertainty. A 0 ohm value(no calibration) can only be achieved if the OCD impedance is 18 ohms +/- 0.75 ohms under nominal conditions.

Output Slew rate load:



7. DRAM output slew rate specification applies to 400Mhz speed bins.
8. Timing skew due to DRAM output slew rate mis-match between DQS / $\overline{DQS}$ and associated DQs is included in tDQSQ and tQHS specification.

5.4 IDD Specifications & Test Conditions

IDD Specifications(max)

Symbol		25C	20L	Units
		400Mhz	500Mhz	
IDD0		95	105	mA
IDD1		120	130	mA
IDD2P		10	10	mA
IDD2Q		32	35	mA
IDD2N		45	50	mA
IDD3P	F	25	25	mA
	S	12	12	mA
IDD3N		55	65	mA
IDD4W		230	300	mA
IDD4R		215	250	mA
IDD5		170	180	mA
IDD6	Normal	10	10	mA
IDD7 (1KB)		290	300	mA

IDD Test Conditions

(IDD values are for full operating range of Voltage and Temperature, Notes 1-5)

Symbol	Conditions		Units
IDD0	**Operating one bank active-precharge current**; ^{t}CK = $^{t}CK(IDD)$, ^{t}RC = $^{t}RC(IDD)$, ^{t}RAS = ^{t}RAS min(IDD) ; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands;Address bus inputs are SWITCHING;Data bus inputs are SWITCHING		mA
IDD1	**Operating one bank active-read-precharge current** ; IOUT = 0mA;BL = 4, CL = CL(IDD), AL = 0; ^{t}CK = $^{t}CK(IDD)$, ^{t}RC = ^{t}RC (IDD), ^{t}RAS = $^{t}RASmin(IDD)$, ^{t}RCD = $^{t}RCD(IDD)$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands ; Address bus inputs are SWITCHING ; Data pattern is same as IDD4W		mA
IDD2P	**Precharge power-down current** ; All banks idle ; ^{t}CK = $^{t}CK(IDD)$; CKE is LOW ; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		mA
IDD2Q	**Precharge quiet standby current**;All banks idle; ^{t}CK = $^{t}CK(IDD)$;CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		mA
IDD2N	**Precharge standby current**; All banks idle; ^{t}CK = $^{t}CK(IDD)$; CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA
IDD3P	**Active power-down current**; All banks open; ^{t}CK = $^{t}CK(IDD)$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MR(12) = 0	mA
		Slow PDN Exit MR(12) = 1	mA
IDD3N	**Active standby current**; All banks open; ^{t}CK = $^{t}CK(IDD)$, ^{t}RAS = $^{t}RASmax(IDD)$, ^{t}RP =$^{t}RP(IDD)$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA
IDD4W	**Operating burst write current**; All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; ^{t}CK = $^{t}CK(IDD)$, ^{t}RAS = $^{t}RASmax(IDD)$, ^{t}RP = $^{t}RP(IDD)$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA
IDD4R	**Operating burst read current**; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; ^{t}CK = $^{t}CK(IDD)$, ^{t}RAS = $^{t}RASmax(IDD)$, ^{t}RP = $^{t}RP(IDD)$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING;; Data pattern is same as IDD4W		mA
IDD5B	**Burst refresh current**; ^{t}CK = $^{t}CK(IDD)$; Refresh command at every $^{t}RFC(IDD)$ interval; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA
IDD6	**Self refresh current**; CK and $\overline{CK}$ at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING		mA
IDD7	**Operating bank interleave read current**; All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = $^{t}RCD(IDD)$-1*$^{t}CK(IDD)$; ^{t}CK = $^{t}CK(IDD)$, ^{t}RC = $^{t}RC(IDD)$, ^{t}RRD = $^{t}RRD(IDD)$, ^{t}RCD = 1*$^{t}CK(IDD)$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R; - Refer to the following page for detailed timing conditions		mA

Note :

1. VDDQ = 1.8 +/- 0.1V ; VDD = 1.8 +/- 0.1V
2. IDD specifications are tested after the device is properly initialized
3. Input slew rate is specified by AC Parametric Test Condition
4. IDD parameters are specified with ODT disabled.
5. Data bus consists of DQ, DM, DQS, $\overline{\text{DQS}}$, RDQS, $\overline{\text{RDQS}}$, LDQS, $\overline{\text{LDQS}}$, UDQS, and $\overline{\text{UDQS}}$. IDD values must be met with all combinations of EMR bits 10 and 11.
6. For 400Mhz testing, tCK in the Conditions should be interpreted as tCK(avg).
7. Definitions for IDD
   LOW is defined as Vin $\leq$ VILAC(max)
   HIGH is defined as Vin $\geq$ VIHAC(min)
   STABLE is defined as inputs stable at a HIGH or LOW level
   FLOATING is defined as inputs at VREF = VDDQ/2
   SWITCHING is defined as: inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per clock) for DQ signals not including masks or strobes.

IDD Testing Parameters

For purposes of IDD testing, the following parameters are to be utilized.

Parameter	25C	20L	Units
CL(IDD)	6	7	tCK
^{t}RCD(IDD)	15	15	ns
^{t}RC(IDD)	60	60	ns
^{t}RRD(IDD)	10	10	ns
^{t}CK(IDD)	2.5	2	ns
^{t}RASmin(IDD)	45	45	ns
^{t}RASmax(IDD)	70k	70k	ns
^{t}RP(IDD)	15	15	ns
^{t}RFC(IDD)	127.5	127.5	ns

Detailed IDD7

The detailed timings are shown below for IDD7. Changes will be required if timing parameter changes are made to the specification.
Legend: A = Active; RA = Read with Autoprecharge; D = Deselect

IDD7: Operating Current: All Bank Interleave Read operation

All banks are being interleaved at minimum ^{t}RC(IDD) without violating ^{t}RRD(IDD) and tFAW(IDD) using a burst length of 4. Control and address bus inputs are STABLE during DESELECTs. IOUT = 0mA

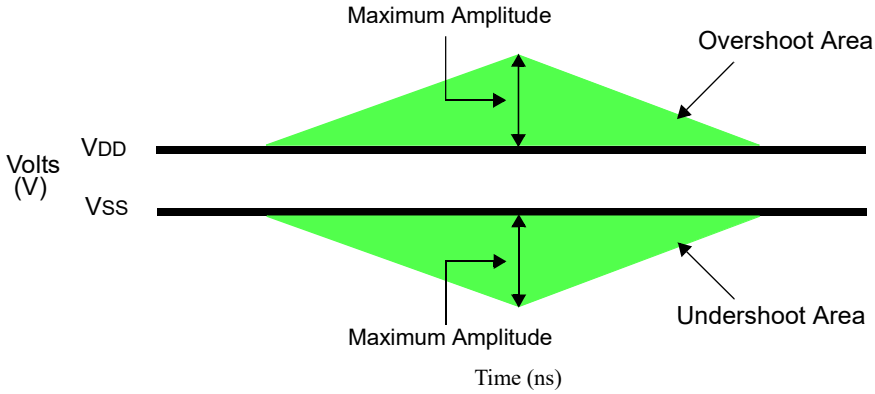
5.5. Input/Output Capacitance

Parameter	Symbol	400/500Mhz		Units
		Min	Max	
Input capacitance, CK and $\overline{CK}$	CCK	1.0	2.0	pF
Input capacitance delta, CK and $\overline{CK}$	CDCK	x	0.25	pF
Input capacitance, all other input-only pins	CI	1.0	1.75	pF
Input capacitance delta, all other input-only pins	CDI	x	0.25	pF
Input/output capacitance, DQ, DM, DQS, $\overline{DQS}$	CIO	2.5	3.5	pF
Input/output capacitance delta, DQ, DM, DQS, $\overline{DQS}$	CDIO	x	0.5	pF

5.6 Overshoot/Undershoot Specification

AC Overshoot/Undershoot Specification for Address and Control Pins A0-A12, BA0-BA2, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE, ODT

Parameter	Specification
Maximum peak amplitude allowed for overshoot area (See Figure 1):	0.9V
Maximum peak amplitude allowed for undershoot area (See Figure 1):	0.9V
Maximum overshoot area above VDD (See Figure1).	0.45 V-ns
Maximum undershoot area below VSS (See Figure 1).	0.45 V-ns



AC Overshoot/Undershoot Specification for Clock, Data, Strobe, and Mask Pins DQ, DQS, DM, CK, CK

Parameter	Specification
Maximum peak amplitude allowed for overshoot area (See Figure 2):	0.9V
Maximum peak amplitude allowed for undershoot area (See Figure 2):	0.9V
Maximum overshoot area above VDDQ (See Figure 2).	0.23 V-ns
Maximum undershoot area below VSSQ (See Figure 2).	0.23 V-ns

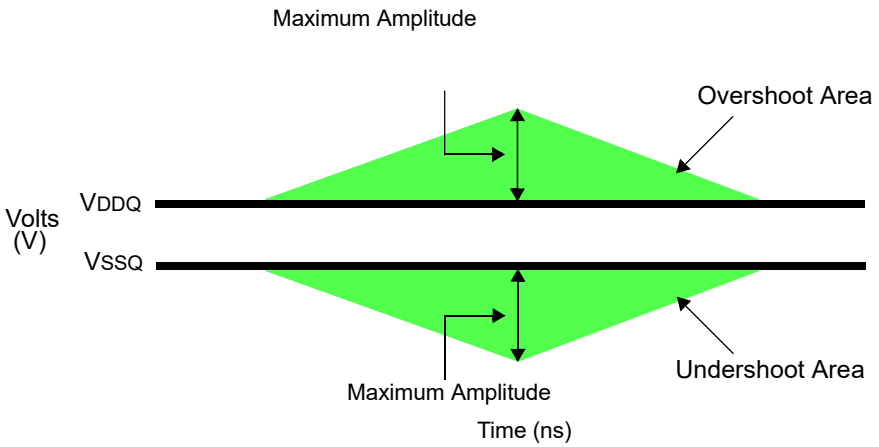


Figure 2: AC Overshoot and Undershoot Definition for Clock, Data, Strobe, and Mask Pins

Power and ground clamps are required on the following input only pins:

1. BA0-BA2
2. A0-A12
3. $\overline{RAS}$
4. $\overline{CAS}$
5. $\overline{WE}$
6. $\overline{CS}$
7. ODT
8. CKE

V-I Characteristics table for input only pins with clamps

Voltage across clamp(V)	Minimum Power Clamp Current (mA)	Minimum Ground Clamp Current (mA)
0.0	0	0
0.1	0	0
0.2	0	0
0.3	0	0
0.4	0	0
0.5	0	0
0.6	0	0
0.7	0	0
0.8	0.1	0.1
0.9	1.0	1.0
1.0	2.5	2.5
1.1	4.7	4.7
1.2	6.8	6.8
1.3	9.1	9.1
1.4	11.0	11.0
1.5	13.5	13.5
1.6	16.0	16.0
1.7	18.2	18.2
1.8	21.0	21.0

6. Electrical Characteristics & AC Timing Specification

6.1 Refresh Parameters by Device Density

(T_{OPER}; V_{DDQ} = 1.8 +/- 0.1V; V_{DD} = 1.8 +/- 0.1V)

Parameter	Symbol		1Gb	Units	Notes
Refresh to Active/Refresh command time	tRFC		127.5	ns	1
Average periodic refresh interval	tREFI	0 ℃ ≤ T_{CASE} ≤ 85℃	7.8	us	1
		85 ℃ ≤ T_{CASE} ≤ 95℃	3.9	us	

Note :

1: If refresh timing is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.

2. This is an optional feature. For detailed information, please refer to "operating temperature condition" in this data sheet.

6.2 DDR2 SDRAM speed bins and tRCD, tRP and tRC for corresponding bin

Speed	500Mhz	400Mhz	300Mhz	200Mhz	100Mhz	Units	Notes
Parameter	min	min	min	min	min		
Bin(CL-tRCD-tRP)	7-7-7	6-6-6	5-5-5	3-3-3	3-2-2		
CAS Latency	7	6	5	3	3	tCK	
tRCD	15	15	15	15	20	ns	
tRP*1	15	15	15	15	20	ns	
tRAS	45	45	45	45	50	ns	2
tRC	60	60	60	60	60	ns	

Note :

* Paramters' value of each speed bin except for 400Mhz is only for the reference data.

1. 8 bank device Precharge All Allowance : tRP for a Precharge All command for an 8 Bank device will equal to tRP+1*tCK, where tRP are the values for a single bank Precharge, which are shown in the table above.

2. Refer to Specific Notes 3.

6.3 Timing Parameters by Speed grade

Parameter	Symbol	20L		25C		Unit	Note
		min	max	min	max		
DQ output access time from CK/$\overline{CK}$	tAC	-350	+350	-400	+400	ps	
DQS output access time from CK/$\overline{CK}$	tDQSCK	-300	+300	-350	+350	ps	
CK HIGH pulse width	tCH(avg)	0.45	0.55	0.45	0.55	tCK(avg)	
CK LOW pulse width	tCL(avg)	0.45	0.55	0.45	0.55	tCK(avg)	
CK half period	tHP	min(tCL(abs), tCH(abs))	-	min(tCL(abs), tCH(abs))	-	ps	
Clock cycle time, CL=x	tCK(avg)	2000	8000	2500	8000	ps	
DQ and DM input setup time	tDS(base)	50	-	50	-	ps	6,7,8
DQ and DM input hold time	tDH(base)	125	-	125	-	ps	6,7,8
Control & Address input pulse width for each input	tIPW	0.6	-	0.6	-	tCK(avg)	
DQ and DM input pulse width for each input	tDIPW	0.35	-	0.35	-	tCK(avg)	
Data-out high-impedance time from CK/$\overline{CK}$	tHZ	-	tAC max	-	tAC max	ps	18
DQS low-impedance time from CK/$\overline{CK}$	tLZ(DQS)	tAC min	tAC max	tAC min	tAC max	ps	18
DQ low-impedance time from CK/$\overline{CK}$	tLZ(DQ)	2*tAC min	tAC max	2*tAC min	tAC max	ps	18
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	-	200	-	200	ps	13
DQ hold skew factor	tQHS	-	300	-	300	ps	
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	-	tHP - tQHS	-	ps	
First DQS latching transition to associated clock edge	tDQSS	- 0.25	+ 0.25	- 0.25	+ 0.25	tCK(avg)	
DQS input HIGH pulse width	tDQSH	0.35	-	0.35	-	tCK(avg)	
DQS input LOW pulse width	tDQSL	0.35	-	0.35	-	tCK(avg)	
DQS falling edge to CK setup time	tDSS	0.2	-	0.2	-	tCK(avg)	
DQS falling edge hold time from CK	tDSH	0.2	-	0.2	-	tCK(avg)	
Mode register set command cycle time	tMRD	2	-	2	-	tCK(avg)	
Write preamble	tWPRE	0.35	-	0.35	-	tCK(avg)	
Write postamble	tWPST	0.4	0.6	0.4	0.6	tCK(avg)	10
Address and control input setup time	tIS(base)	300	-	400	-	ps	5,7,9
Address and control input hold time	tIH(base)	300	-	400	-	ps	5,7,9
Read preamble	tRPRE	0.9	1.1	0.9	1.1	tCK(avg)	
Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK(avg)	
Activate to precharge command	tRAS	45	70000	45	70000	ns	3
Active to active command period for 2KB page size products (x16)	tRRD	10	-	10	-	ns	4
Four Active Window for 2KB page size products	tFAW	45	-	45	-	ns	
$\overline{CAS}$ to $\overline{CAS}$ command delay	tCCD	2		2		nCK	
Write recovery time	tWR	14	-	15	-	ns	
Auto precharge write recovery + precharge time	tDAL	WR+tnRP	-	WR+tnRP	-	nCK	

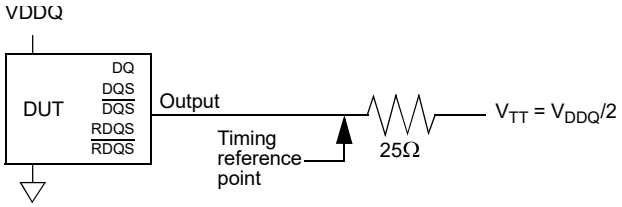
-Continued-

Parameter	Symbol	20L		25C		Unit	Notes
		min	max	min	max		
Internal write to read command delay	tWTR	7.5	-	7.5	-	ns	
Internal read to precharge command delay	tRTP	7.5		7.5		ns	3
Exit self refresh to a non-read command	tXSNR	tRFC + 10		tRFC + 10		ns	
Exit self refresh to a read command	tXSRD	200	-	200	-	nCK	
Exit precharge power down to any non-read command	tXP	2	-	2	-	nCK	
Exit active power down to read command	tXARD	2		2		nCK	1
Exit active power down to read command (Slow exit, Lower power)	tXARDS	8 - AL		8 - AL		nCK	1, 2
CKE minimum pulse width (HIGH and LOW pulse width)	tCKE	3		3		nCK	
ODT turn-on delay	tAOND	2	2	2	2	nCK	16
ODT turn-on	tAON	tAC(min)	tAC(max) +0.7	tAC(min)	tAC(max) +0.7	ns	6,16
ODT turn-on(Power-Down mode)	tAONPD	tAC(min) +2	2tCK(avg)+ tAC(max)+1	tAC(min) +2	2tCK(avg)+ tAC(max)+1	ns	
ODT turn-off delay	tAOFD	2.5	2.5	2.5	2.5	nCK	17
ODT turn-off	tAOF	tAC(min)	tAC(max) +0.6	tAC(min)	tAC(max) +0.6	ns	17
ODT turn-off (Power-Down mode)	tAOFPD	tAC(min) +2	2.5tCK(avg)+ tAC(max)+1	tAC(min) +2	2.5tCK(avg)+ tAC(max)+1	ns	
ODT to power down entry latency	tANPD	3		3		nCK	
ODT power down exit latency	tAXPD	8		8		nCK	
OCD drive mode output delay	tOIT	0	12	0	12	ns	
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK(av) +tIH		tIS+tCK(av) +tIH		ns	15

General notes, which may apply for all AC parameters

1. DDR2 SDRAM AC timing reference load

The following figure represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics).



AC Timing Reference Load

The output timing reference voltage level for single ended signals is the crosspoint with VTT. The output timing reference voltage level for differential signals is the crosspoint of the true (e.g. DQS) and the complement (e.g. $\overline{DQS}$) signal.

2. Slew Rate Measurement Levels

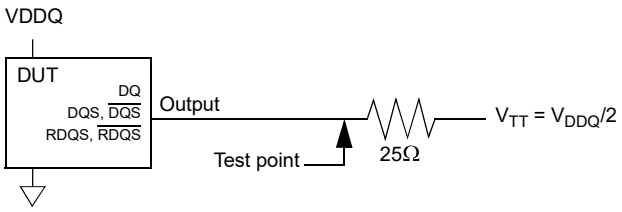
a. Output slew rate for falling and rising edges is measured between VTT - 250 mV and VTT + 250 mV for single ended signals. For differential signals (e.g. DQS - $\overline{DQS}$) output slew rate is measured between DQS - $\overline{DQS}$ = -500 mV and DQS - $\overline{DQS}$ = +500mV. Output slew rate is guaranteed by design, but is not necessarily tested on each device.

b. Input slew rate for single ended signals is measured from dc-level to ac-level: from VREF - 125 mV to VREF + 250 mV for rising edges and from VREF + 125 mV and VREF - 250 mV for falling edges. For differential signals (e.g. CK - $\overline{CK}$) slew rate for rising edges is measured from CK - $\overline{CK}$ = -250 mV to CK - $\overline{CK}$ = +500 mV (+250mV to -500 mV for falling egdes).

c. VID is the magnitude of the difference between the input voltage on CK and the input voltage on $\overline{CK}$, or between DQS and $\overline{DQS}$ for differential strobe.

3. DDR2 SDRAM output slew rate test load

Output slew rate is characterized under the test conditions as shown below.



Slew Rate Test Load

4. Differential data strobe

DDR2 SDRAM pin timings are specified for either single ended mode or differential mode depending on the setting of the EMR "Enable DQS" mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timings are measured is mode dependent. In single ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at VREF. In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, $\overline{DQS}$. This distinction in timing methods is guaranteed by design and characterization. Note that when differential data strobe mode is disabled via the EMR, the complementary pin, $\overline{DQS}$, must be tied externally to VSS through a 20 Ω to 10 KΩ resistor to insure proper operation.

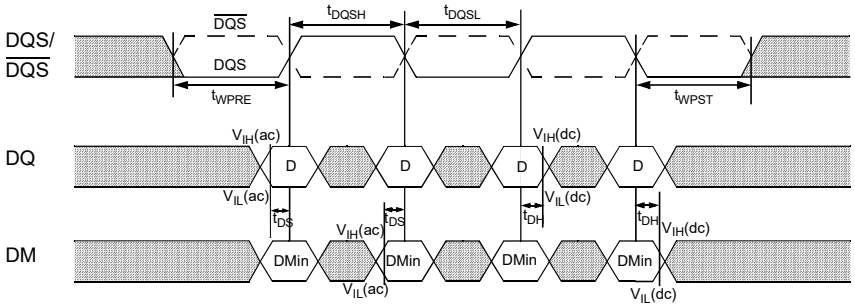


Figure -- Data input (write) timing

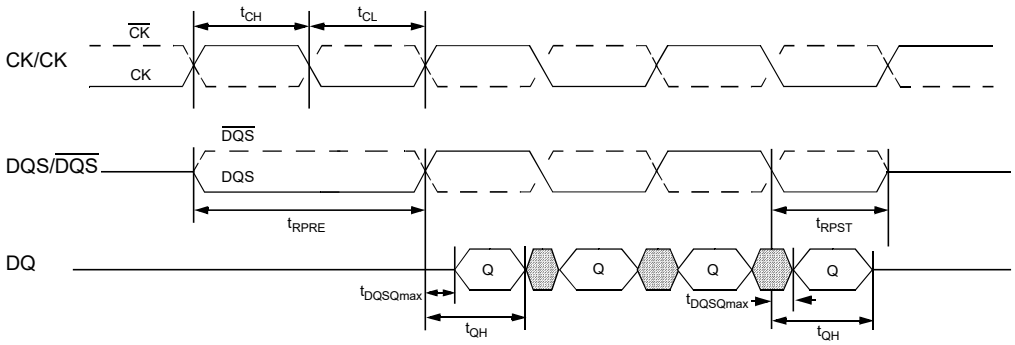


Figure -- Data output (read) timing

5. AC timings are for linear signal transitions. See System Derating for other signal transitions.

6. All voltages referenced to VSS.

7. These parameters guarantee device behavior, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.

8. Tests for AC timing, IDD, and electrical (AC and DC) characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.

Specific Notes for dedicated AC parameters

1. User can choose which active power down exit timing to use via MRS(bit 12). tXARD is expected to be used for fast active power down exit timing. tXARDS is expected to be used for slow active power down exit timing where a lower power value is defined by each vendor data sheet.

2. AL = Additive Latency

3. This is a minimum requirement. Minimum read to precharge timing is AL + BL/2 providing the tRTP and tRAS(min) have been satisfied.

4. A minimum of two clocks (2 * tCK or 2 * nCK) is required irrespective of operating frequency

5. Timings are specified with command/address input slew rate of 1.0 V/ns. See System Derating for other slew rate values.

6. Timings are guaranteed with DQs, DM, and DQS's(DQS/RDQS in singled ended mode) input slew rate of 1.0 V/ns. See System Derating for other slew rate values.

7. Timings are specified with CK/$\overline{CK}$ differential slew rate of 2.0 V/ns. Timings are guaranteed for DQS signals with a differential slew rate of 2.0 V/ns in differential strobe mode and a slew rate of 1V/ns in single ended mode. See System Derating for other slew rate values.

8. tDS and tDH derating

tDS, tDH Derating Values for 400Mhz (ALL units in 'ps', Note 1 applies to entire Table)																	
		DQS, $\overline{DQS}$ Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
DQ Slew rate V/ns	2.0	100	45	100	45	100	45	-	-	-	-	-	-	-	-	-	-
	1.5	67	21	67	21	67	21	79	33	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	12	12	24	24	-	-	-	-	-	-
	0.9	-	-	-5	-14	-5	-14	7	-2	19	10	31	22	-	-	-	-
	0.8	-	-	-	-	-13	-31	-1	-19	11	-7	23	5	35	17	-	-
	0.7	-	-	-	-	-	-	-10	-42	2	-30	14	-18	26	-6	38	6
	0.6	-	-	-	-	-	-	-	-	-10	-59	2	-47	14	-35	26	-23

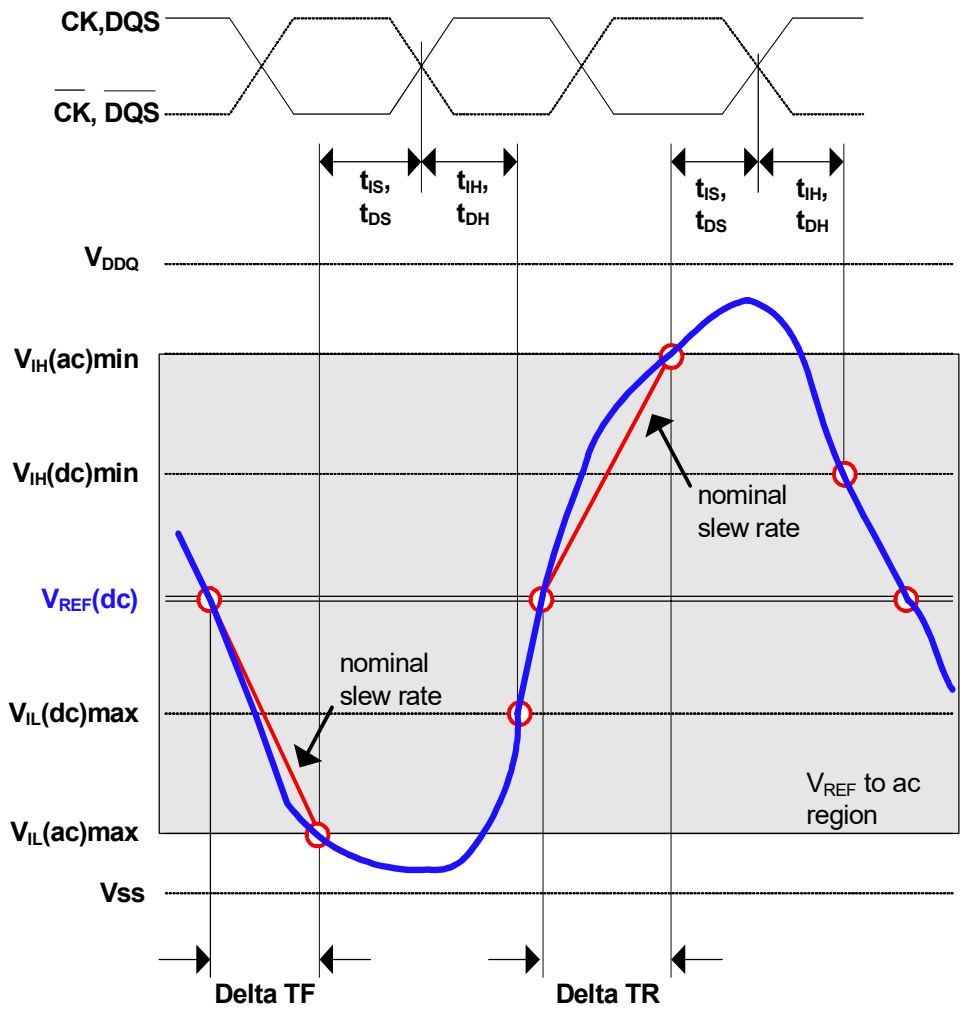
1) For all input signals the total tDS(setup time) and tDH(hold time) required is calculated by adding the datasheet value to the derating value listed in Table x.

Setup(tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of Vih(ac)min. Setup(tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of Vil(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded ' VREF(dc) to ac region', use nominal slew rate for derating value(see Fig a.) If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF(dc) to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value(see Fig b.)

Hold(tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of Vil(dc) max and the first crossing of VREF(dc). Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of Vih(dc) min and the first crossing of VREF(dc). If the actual signal is always later than the nominal slew rate line anywhere between shaded 'dc to VREF(dc) region', the slew rate of a tangent line to the actual signal from the dc level to VREF(dc) level is used for derating value(see Fig c.) If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to VREF(dc) region', the slew rate of a tangent line to the actual signal from the dc level to VREF(dc) level is used for derating value(see Fig d.)

Although for slow slew rates the total setup time might be negative(i.e. a valid input signal will not have reached VIH/IL(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(ac).
For slew rate in between the values listed in table x, the derating valued may obtained by linear interpolation.
These values are typically not subject to production test. They are verified by design and characterization.

Fig. a. Illustration of nominal slew rate for tIS,tDS



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF}(dc)-V_{IL}(ac)max}{\text{Delta TF}} \qquad \text{Setup Slew Rate Rising Signal} = \frac{V_{IH}(ac)min-V_{REF}(dc)}{\text{Delta TR}}$$

Fig. b. Illustration of tangent line for tIS,tDS

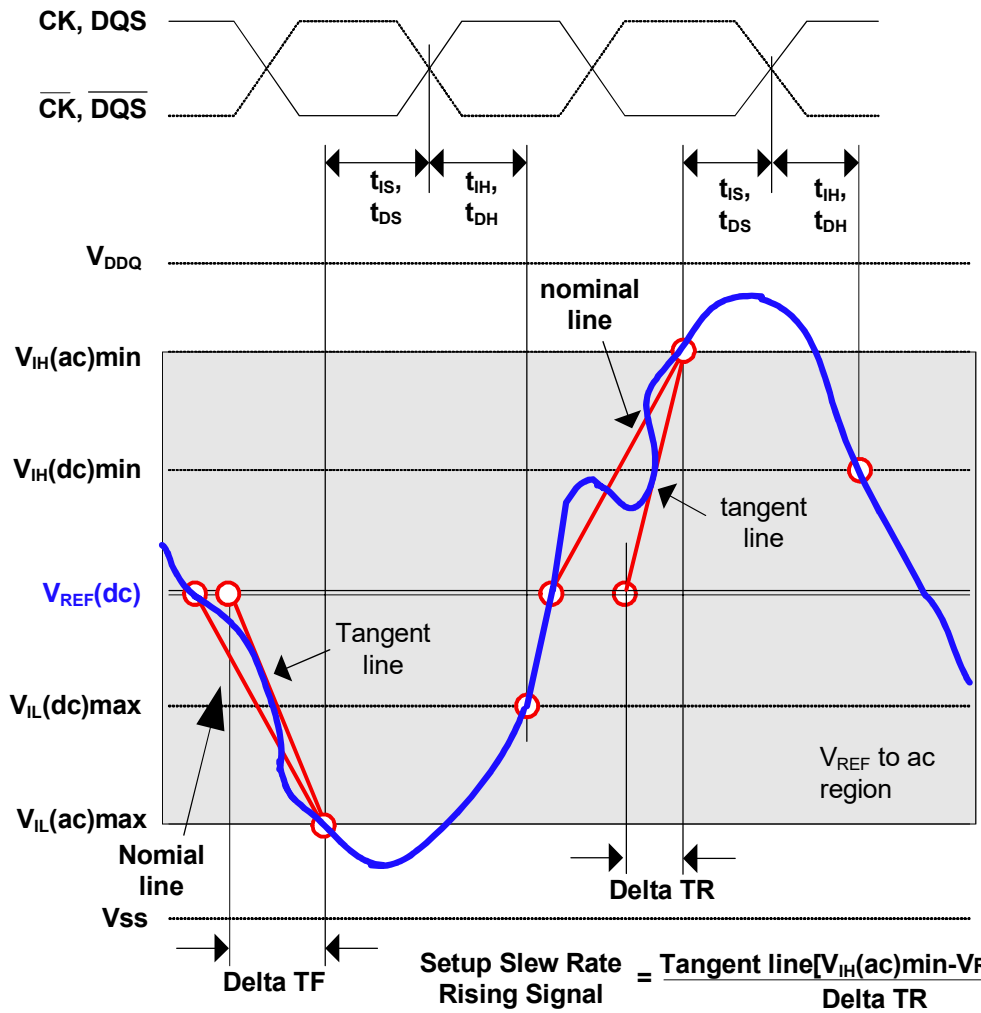
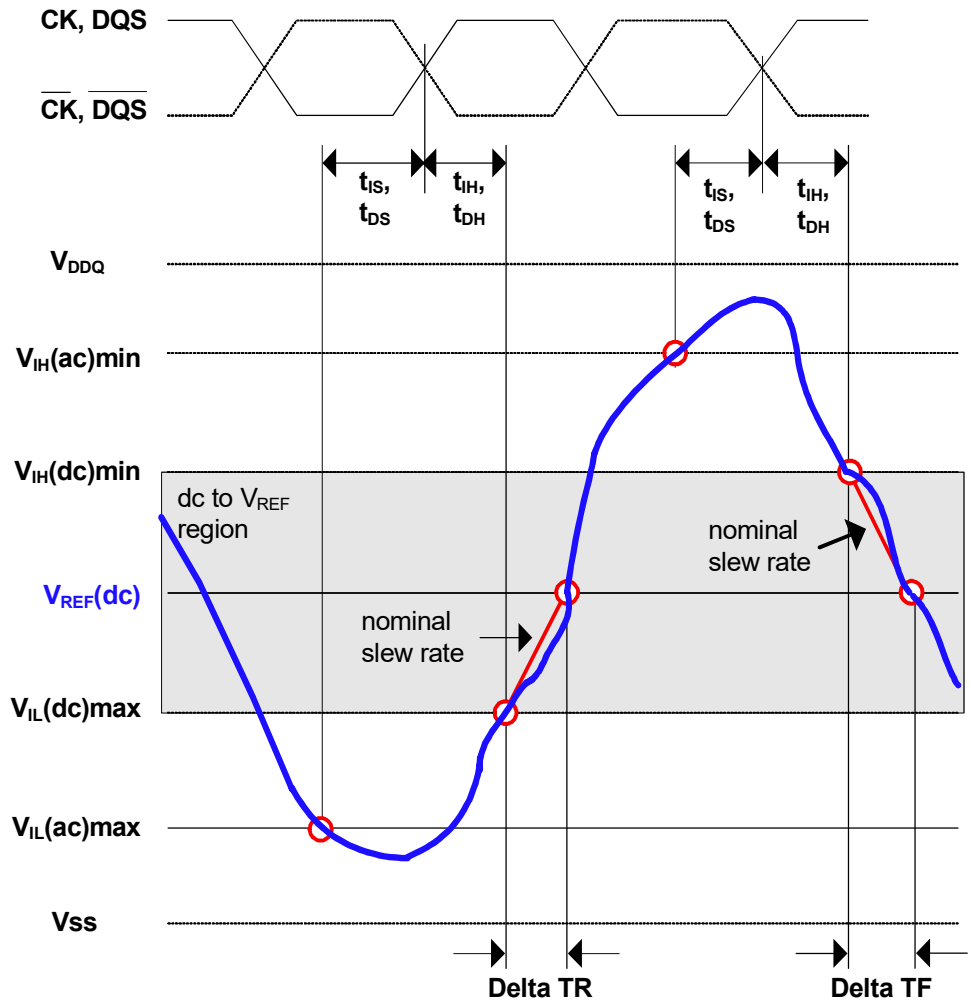
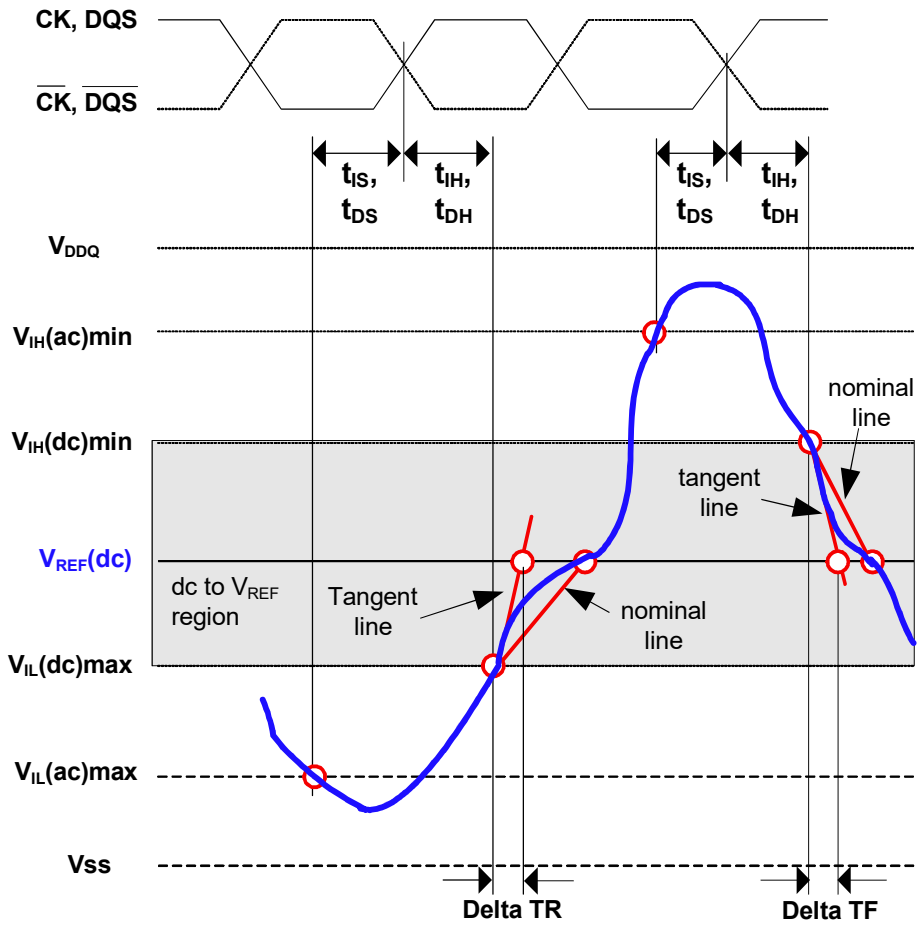


Fig. c. Illustration of nominal line for tIH, tDH



$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF}(dc)-V_{IL}(dc)max}{\text{Delta TR}} \qquad \text{Hold Slew Rate Falling Signal} = \frac{V_{IH}(dc)min - V_{REF}(dc)}{\text{Delta TF}}$$

Fig. d. Illustration of tangent line for tIH , tDH



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{Tangent line}[V_{REF}(dc)-V_{IL}(ac)max]}{\text{Delta TR}}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{Tangent line}[V_{IH}(ac)min-V_{REF}(dc)]}{\text{Delta TF}}$$

9. tIS and tIH (input setup and hold) derating

tIS, tIH Derating Values for 400Mhz									
		CK, $\overline{CK}$ Differential Slew Rate							
		2.0 V/ns		1.5 V/ns		1.0 V/ns			
		△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	Units	Notes
Command / Address Slew rate(V/ns)	4.0	+15	+94	+180	+124	+210	+154	ps	1
	3.5	+143	+89	+173	+119	+203	+149	ps	1
	3.0	+133	+83	+163	+113	+193	+143	ps	1
	2.5	+120	+75	+150	+105	+180	+135	ps	1
	2.0	+100	+45	+130	+75	+150	+105	ps	1
	1.5	+67	+21	+97	+51	+127	+81	ps	1
	1.0	0	0	+30	+30	+60	+60	ps	1
	0.9	-5	-14	+25	+16	+55	+46	ps	1
	0.8	-13	-31	+17	-1	+47	+29	ps	1
	0.7	-22	-54	+8	-24	+38	+6	ps	1
	0.6	-34	-83	-4	-53	+26	-23	ps	1
	0.5	-60	-125	-30	-95	0	-65	ps	1
	0.4	-100	-188	-70	-158	-40	-128	ps	1
	0.3	-168	-292	-138	-262	-108	-232	ps	1
	0.25	-200	-375	-170	-345	-140	-315	ps	1
	0.2	-325	-500	-395	-470	-265	-440	ps	1
	0.15	-517	-708	-487	-678	-457	-648	ps	1
	0.1	-1000	-1125	-970	-1095	-940	-1065	ps	1

1) For all input signals the total tIS(setup time) and tIH(hold) time) required is calculated by adding the datasheet value to the derating value listed in above Table.

Setup(tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of V_{REF}(dc) and the first crossing of V_{IH}(ac)min. Setup(tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of V_{REF}(dc) and the first crossing of V_{IL}(ac)max. If the actual signal is always earlier than the nominal slew rate for line between shaded 'V_{REF}(dc) to ac region', use nominal slew rate for derating value(see fig a.) If the actual signal is later than the nominal slew rate line anywhere between shaded 'V_{REF}(dc) to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value(see Fig b.)

Hold(tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(dc)max and the first crossing of V_{REF}(dc). Hold(tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of V_{REF}(dc). If the actual signal is always later than the nominal slew rate line between shaded 'dc to V_{REF}(dc) region', use nominal slew rate for derating value(see Fig.c) If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to V_{REF}(dc) region', the slew rate of a tangent line to the actual signal from the dc level to V_{REF}(dc) level is used for derating value(see Fig d.)

Although for slow rates the total setup time might be negative(i.e. a valid input signal will not have reached $V_{IH/IL}$(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL}$(ac).

For slew rates in between the values listed in table, the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

10. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.

11. MIN (t CL, t CH) refers to the smaller of the actual clock LOW time and the actual clock HIGH time as provided to the device (i.e. this value can be greater than the minimum specification limits for t CL and t CH). For example, t CL and t CH are = 50% of the period, less the half period jitter (t JIT(HP)) of the clock source, and less the half period jitter due to crosstalk (t JIT(crosstalk)) into the clock traces.

12. t QH = t HP – t QHS, where:
tHP = minimum half clock period for any given cycle and is defined by clock HIGH or clock LOW (tCH,tCL).
tQHS accounts for:
1) The pulse duration distortion of on-chip clock circuits; and
2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.

13. tDQSQ: Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output slew rate mismatch between DQS/ $\overline{DQS}$ and associated DQ in any given cycle.

14. t DAL = (nWR) + (tRP/tCK):
For each of the terms above, if not already an integer, round to the next highest integer. tCK refers to the application clock period. nWR refers to the t WR parameter stored in the MR.

15. The clock frequency is allowed to change during self–refresh mode or precharge power-down mode.
In case of clock frequency change during precharge power-down.

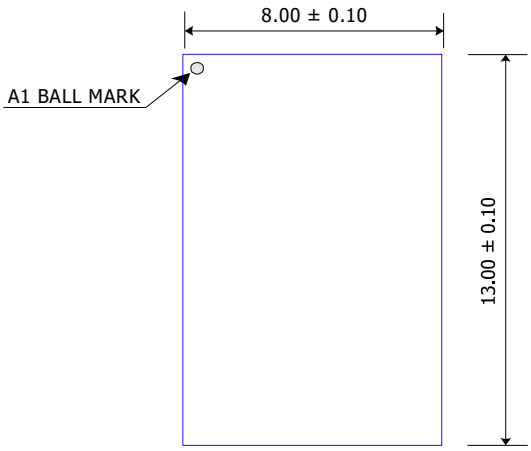
16. ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on.
ODT turn on time max is when the ODT resistance is fully on. Both are measured from tAOND.

17. ODT turn off time min is when the device starts to turn off ODT resistance.
ODT turn off time max is when the bus is in high impedance. Both are measured from tAOFD.

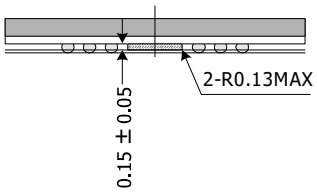
18. tHZ and tLZ transitions occur in the same access time as valid data transitions. Thesed parameters are referenced to a specific voltage level which specifies when the device output is no longer driving(tHZ), or begins driving (tLZ). Below figure shows a method to calculate the point when device is no longer driving (tHZ), or begins driving (tLZ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistenet.

7. Package Dimension(x16)

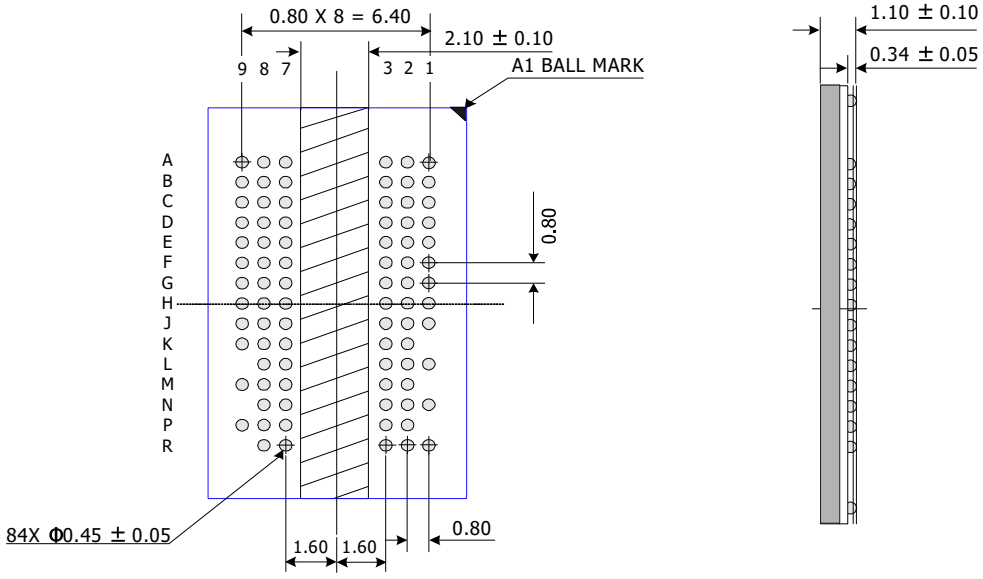
84Ball Fine Pitch Ball Grid Array Outline



< Top View>



< SIDE View>



< Bottom View>

Note: All dimensions are in millimeters.