AL2230S

Single Chip Transceiver for 2.4GHz 802.11b/g Applications

(AIROHA)

INDEX

AL2230S – Single Chip Transceiver for 2.4GHz 802.11b/g

Applications

1 Features

- Highly integrated 2.4GHz band transceiver with Direct Conversion architecture
- Receiver with 40dB RF selectable gain range and 60dB baseband variable gain range
- Integrated baseband filters with programmable bandwidth for Transmitter and Receiver
- Three-wire control interface
- Integrate PA with 20dBm output power for 11b and 17dBm for 11g
- Integrate RF detector for APC
- Single-ended LNA input without the need of external balun
- On-chip DC offset correction
- Embedded IQ mismatch calibration
- Small QFN-48 package (7mm×7mm)

2 Description

AL2230S is a highly integrated RF transceiver IC for 2.4GHz band 802.11b/g applications, and combines all functions of the transceiver in a single chip. AL2230S also integrates on-chip PA and PLL to help you to minimize the use of external components to design an RF subsystem.

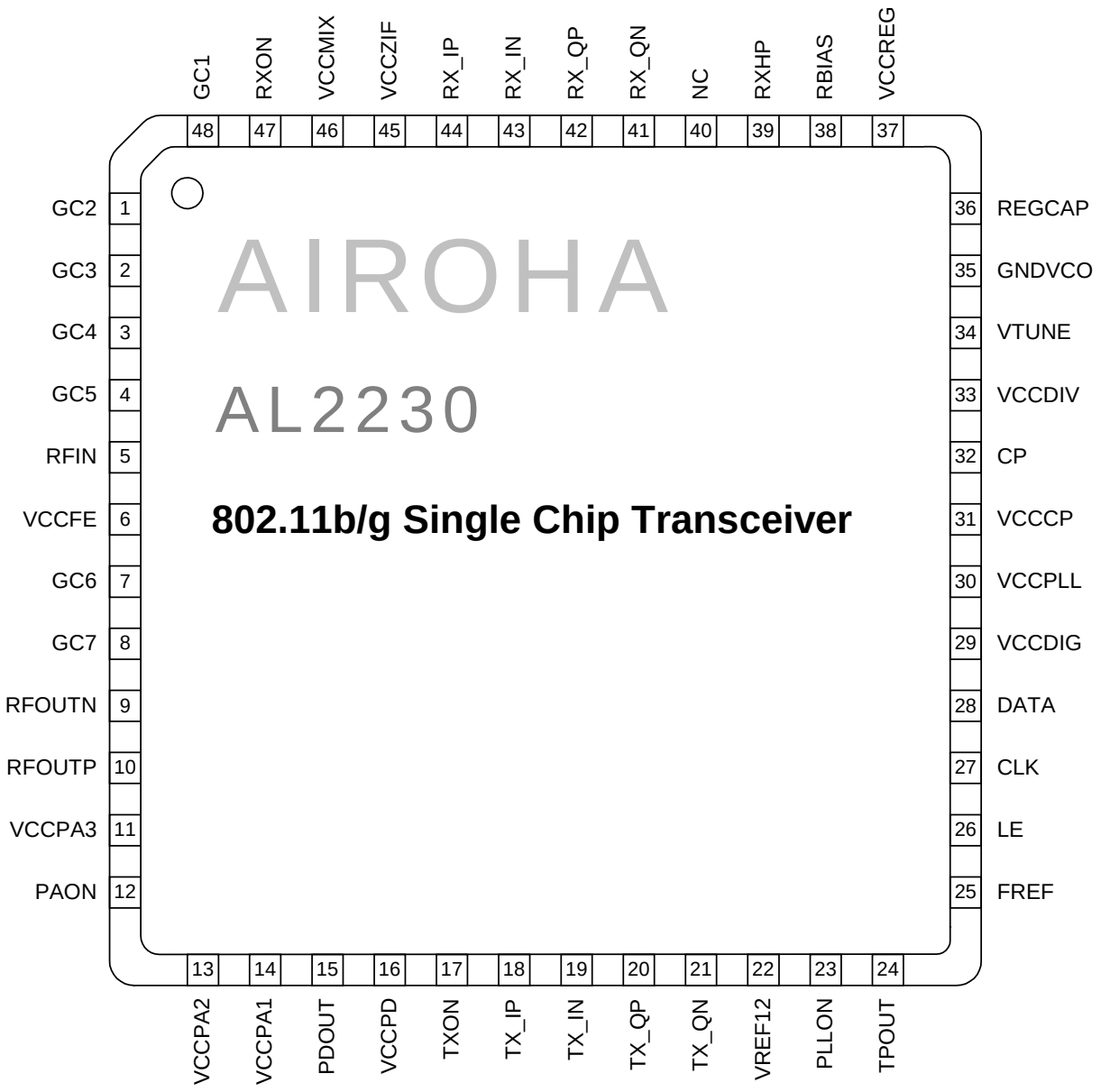
The receive path implements a direct down-conversion architecture to eliminate additional IF filters. It includes a single-ended input Low Noise Amplifier (LNA), a direct down-conversion mixer with DC-offset cancellation, and a variable gain amplifier with a baseband low-pass filter.

The transmitter consists of a direct up-conversion quadrature modulator with a baseband low pass filter, a variable gain amplifier, a power amplifier and a power detector to complete the whole transmit path function.

A power-on calibration procedure is established to correct the TX DC offset and filters mismatch.

These functions are housed in a 48-pin QFN package.

3 Pin Assignment



4 Block Description

4.1 General Description

The AL2230S is a 2.4GHz-band transceiver for 802.11b/g applications. There are five main blocks – power amplifier, transmitter, receiver, synthesizer and three-wire interface.

The control pins: PLLON, TXON, RXON and PAON are responsible for the power control of the chip. The whole chip is powered up when PLLON is set to High, and the synthesizer is enabled at the same time. After the chip powered-up, the transmitter or receiver block is enabled when TXON or RXON being set to High, respectively. The PA block is controlled by the PAON pin independently, irrelative to the state of PLLON.

4.2 Receiver

The receiver implements a direct-conversion architecture, which is composed with two parts: RF front-end and Zero-IF baseband. The RF front-end part comprises a LNA and a quadrature mixer. The ZIF baseband part comprises a low-pass filter (LPF) for channel filtering, a variable gain amplifier (VGA) and a RSSI log amplifier for RSSI output.

At the RF front-end part, the LNA input is single-ended without the need of external balun. The front-end gain could be adjusted through control pins or 3-wire interface, and thus reduce the probability of bit errors caused by poor signal-to-noise ratio.

After the LNA is followed by a quadrature mixer that down-converts the RF signal directly to baseband signal. A direct-conversion architecture is implemented in order to eliminate the external SAW filters.

At the ZIF baseband part, the down-converted baseband signal is first low-pass filtered by the LPF, and then amplified by the VGA. The 3dB bandwidth of the LPF could be set from 7.5MHz to 20MHz through 3-wire interface.

The VGA provides variable gain with 60dB dynamic range, and could be controlled through control pins or 3-wire interface.

The Rx I/Q output are designed to be directly connected (DC-coupled) to I/Q ADC inputs of the baseband IC. The common voltage of RX I/Q outputs is 1.2V.

The RF front-end provides 5dB system noise figure, –17dBm IIP3, and a RF gain step of 22dB/18dB. The baseband provides 60dB gain range from maximum to minimum. The overall voltage gain control range is 100dB.

4.3 Transmitter

The transmitter implements a direct-up-conversion architecture, which comprises a LPF, a modulator and a VGA stage. The TX baseband I/Q interface is designed as differential analog inputs directly connected (DC-coupled) to the I/Q DAC outputs of the baseband IC.

A LPF is implemented to attenuate the second sidelobe of signal spectrum and unwanted oversampling clock or spurious signals. The 3dB bandwidth of the LPF could be set from 10MHz to 30MHz through 3-wire interface.

The VGA provides variable gain with 30dB dynamic range, and could be controlled through control pins or 3-wire interface.

4.4 PA

The gain of the power amplifier can be adjusted via bias current, which is controlled through 3-wire interface. Output power is +20dBm for 11b and +17dBm for 11g.

An on-chip power detector is integrated to measure the output power strength. Power detector samples the peak voltage of the output power and generates a voltage proportional to the output power.

4.5 Synthesizer

The AL2230S includes a fractional-N synthesizer. The reference frequency is fed from an external 20/40MHz oscillator.

5 Absolute Maximum Ratings

AL2230S could be damaged by any stress in excess of the absolute maximum ratings listed below.

ITEM	MIN.	MAX.
Power supply voltage (Vcc)	-0.3V	4.0V
Pin voltage	-0.3V	Vcc + 0.3V
Maximum power dissipation	-	2W
Operating temperature	-40°C	+85°C
Storage temperature	-65°C	+150°C
LNA input level	-	+10 dBm
PA output load mismatch	-	10:1

TABLE 1 Absolute Maximum Ratings

5.1 DC Specifications

Typical values are at VCC=3.3V(PA)/2.8V(TRX), Ta=25 °C unless otherwise specified

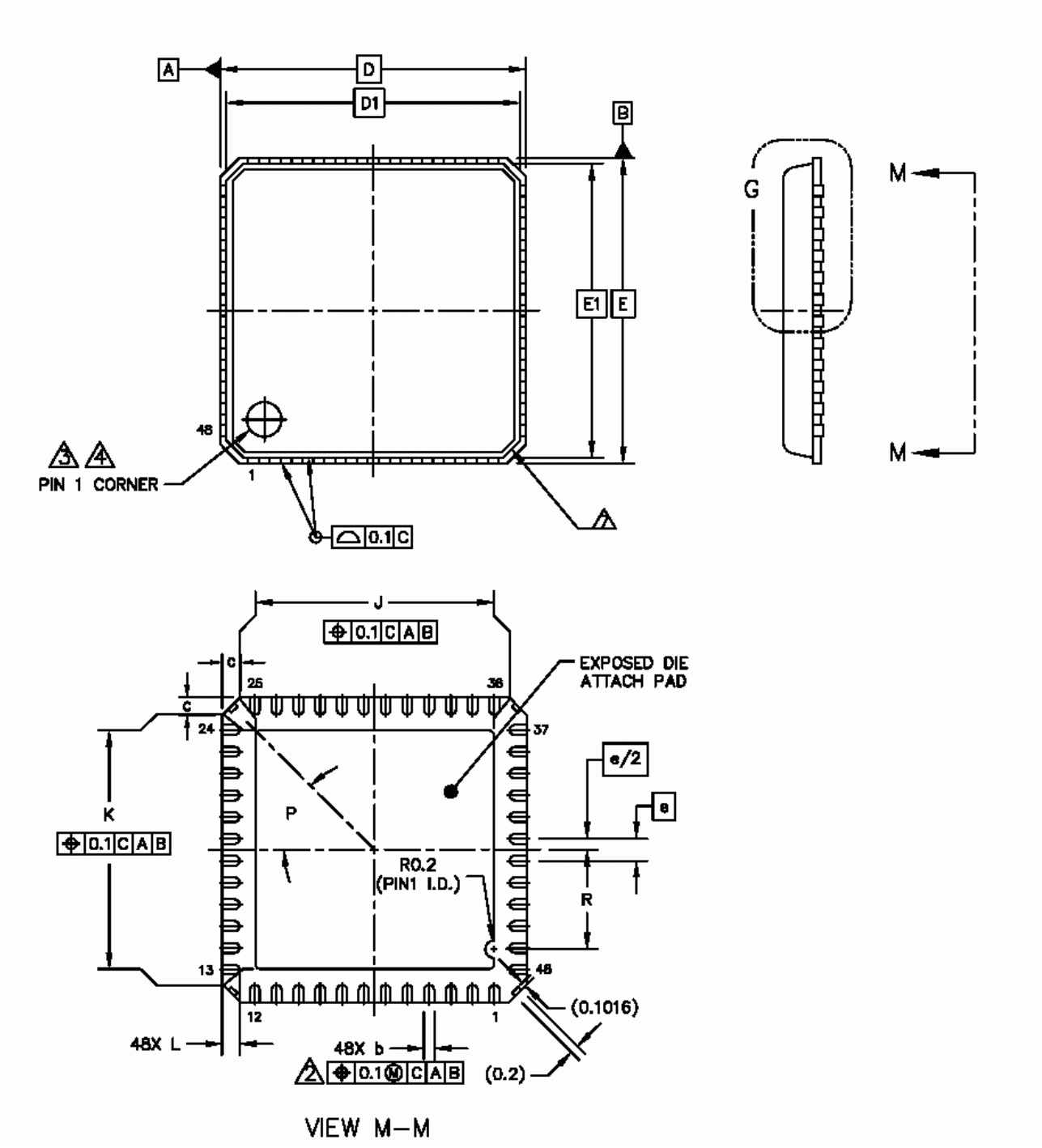
Item	Condition	Min.	Typ.	Max.	Unit
Power supply voltage	Power Amplifier	3	3.3	3.6	V
	Transceiver (V_{DD})		2.8		
Digital input voltage	Logic High (V_{IH})	$0.7V_{DD}$		$V_{DD}+0.3$	V
	Logic Low (V_{IL})	-		$0.3V_{DD}$	
Shut down current	PLLON=L, PD1=PD2=1		5		µA
	PLLON=L, PD1=PD2=0		800		
Standby current	PLLON=H		50		mA
Rx current	PLLON=RXON=H		81		mA
Tx current	PLLON=TXON=H		96		mA
	PLLON=TXON=PAON=H		227 / 249*		

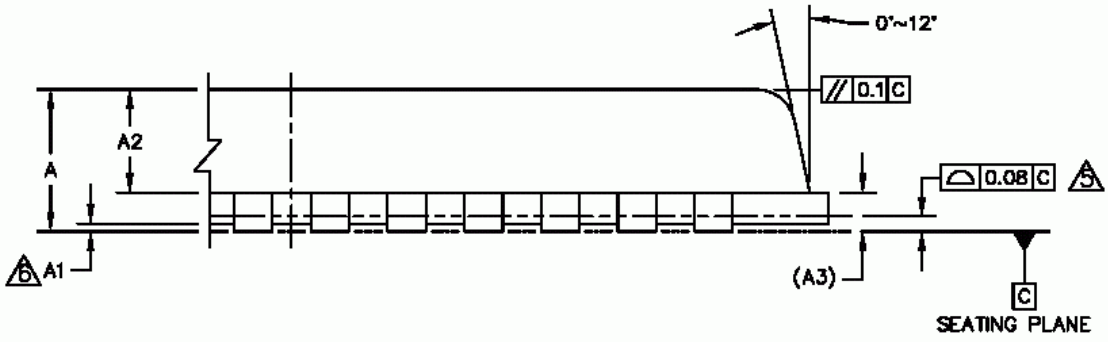
TABLE 2 DC Specifications

*note：227mA under Pout 16dBm OFDM mode, 249mA under Pout 19dBm CCK mode.

6 Package Dimensions

PUNCH QFN 48LD
7x7x0.9 PKG 0.5 PITCH POD





DETAIL G
VIEW ROTATED 90° CLOCKWISE

DIM	MIN	NOM	MAX
A	0.8		0.9
A1	0	0.02	0.05
A2	0.576	0.615	0.654
A3		0.203 REF.	
b	0.18	0.25	0.3
C	0.24	0.42	0.6
D		7 BSC	
D1		6.75 BSC	
E		7 BSC	
E1		6.75 BSC	
e		0.5 BSC	
J	5.37	5.47	5.57
K	5.37	5.47	5.57
L	0.3	0.4	0.5
P		45° REF	
R	2.185	2.285	2.385

NOTES

1. DIE THICKNESS ALLLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
2. DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.2 AND 0.25mm FROM TERMINAL TIP.
3. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
4. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
5. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
6. APPLIED ONLY TO TERMINALS.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

UNIT	DIMENSION AND TOLERANCES	REFERENCE DOCUMENT
MM	ASME Y14.5M	JEDEC-MO-220-F